IMPACT OF FABRICATION PROCESS VARIATIONS ON THE ELECTRICAL PERFORMANCE OF IMPEDANCE CONTROLLED 2 MICRON MULTILAYER REDISTRIBUTION LAYERS (RDL) ON GLASS INTERPOSERS

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To God, my wife, family, and friends.

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LIST OF SYMBOLS

$\alpha_{\text{cond, rough}}$	Attenuation constant for rough surface
$\alpha_{\text{cond, smooth}}$	Attenuation constant for ideal smooth surface
A	Copper area
C	Capacitance per unit length
C_1 or C_2	Partial capacitance per unit length
δ_s	Skin depth
ε_0	Vacuum permittivity
ε_e	Effective dielectric constant
ε_r or Dk	Relative permittivity
F	Faraday constant
G	Conductance per unit length
G_1 or G_2	Partial conductance per unit length
Gap_top or Gap_bottom	Top or bottom gap between signal to ground for CPW
H	Effective dielectric thickness
H_{HJ}	Hammerstad coefficient
I	Copper plating current
l	Ring circumference
λ	Wavelength
K_w	Groisse coefficient
L	Inductance per unit length
M_w	Copper molar mass
μ	Permeability

ω	Angular frequency
ρ	Copper density
σ	Conductivity
σ_c	Modified conductivity
R_a	Average value of surface roughness
R_z	Ten-point mean roughness
R	Resistance per unit length
SF	Hammerstad model scaling factor
tan δ or Df	Loss tangent
T	Copper thickness
t	Copper plating time
W	Transmission line width
W_top or W_bottom	Transmission line top or bottom width
Z_0	Characteristic impedance of transmission line

LIST OF ABBREVIATIONS

2D	Two dimensional
2.5D	Two-and-a-half-dimensional
3D	Three dimensional
ABF	Ajinomoto build-up film
AC	Alternating current
Adv-SLC	Advanced surface laminar circuit
ADS	Advanced design system
AFM	Atomic-force microscopy
APX	Advanced package X
BCB	Benzocyclobutene
BGA	Ball grid array
B-HAST	Biased highly accelerated stress test
BT	Bismaleimide triazine
CCL	Copper clad laminate
CD	Critical dimension
CMP	Chemical mechanical polishing
CO_2	Carbon dioxide
CPU	Central processing unit
CPW	Coplanar waveguide
CTE	Coefficient of thermal expansion
Cu	Copper
DC	Direct current

DFR	Dry-film resist
DOF	Depth of field
DRIE	Deep reactive-ion etch
EM	Electromagnetic
EMIB	Embedded multi-die interconnect bridge
FPGA	Field-programmable gate array
GPU	Graphic processing unit
HBM	High bandwidth memory
HFSS	High frequency structural simulator
IC	Integrated circuit
LGA	Land grid array
MCM	Multi-chip module
NiCr	Nickel-chromium
PID	Photo imageable dielectric
PVD	Physical vapor deposition
PWB	Printed wiring board
RDL	Redistribution layer
RMS	Root mean square
SAP	Semi-additive process
SEM	Scanning electron microscope
Si	Silicon
SLM	Standard liter per minute
SMT	Surface mount technology
SOLT	Short-Open-Load-Through
Ti	Titanium

TOK	Tokyo Ohka Kogyo Co., Ltd
TPV	Through-package via
TSV	Through-silicon via
TTV	Total thickness variation
UV	Ultraviolet
VNA	Vector network analyzer
WLP	Wafer-level packaging

SUMMARY

2.5D interposers integrate logic and memory devices at close proximity and achieve high bandwidths by increasing the density of chip-to-chip interconnections. The 2.5D architecture has become a compelling alternative to 3D IC stacking for the scaling of smart mobile and cloud computing systems. Traditional 2D packaging of individual devices and connecting them at board level cannot achieve high bandwidths due to the limited pitch scaling of board-level interconnections. The current approaches for high-density 2.5D interposers are based on either incrementally extending organic substrates, or silicon carriers with through-silicon vias (TSVs), which utilize back-end of line (BEOL) tools and processes to form multiple re-distribution layers (RDL) at ultra-fine pitch. Organic substrates are limited in scaling to fine pitch by the large via capture pads due to higher dimensional instability, and also by lithographic accuracy due to their non-planar and rough surface. Recent advances in thin film wiring processes have pushed the limits of SAP processes on organic interposers to less than 10 μm lines and spaces. To address the challenges of both silicon and organic, panel-based glass interposers have been demonstrated as a lower cost and higher performance alternative. This research, for the first time, presents a comprehensive study of the impact of re-distribution layer (RDL) process variations on the electrical performance such as 50 ohm impedance for transmission lines down to 3 μm critical dimensions (CD) on glass interposers for 2.5D multi-die interconnections.

The 2D extractor models were established to provide the impedance controlled design rules on glass interposer with available advanced epoxy dry film as well as future

material requirements for 2 μm width and 3 μm thickness microstrip lines and striplines. These 2D extractor models were further analysis with proposed 4 types of process variations for the RLCG parameters and characteristic impedance, providing the process tolerance for different impedance target.

The traditional Semi-Additive Process (SAP) method for multi-layer RDL fabrication was advanced to achieve 2 μm line and space high density routing on glass substrates, closing the gap of the routing density between wafer foundries and package foundries. The photo lithography process with dry film resist (DFR) was optimized by enhancing the adhesion between the DFR and the copper seed layer as well as applying thinner DFR with optimized projection lithography conditions to enable 2 μm RDL scaling technology. Ozone treatment was proposed and tested as a high throughput alternative to traditional oxygen plasma treatment for surface modification and cleaning prior to copper metallization. Copper seed layer etch process was analyzed with advanced etchant to provide design compensation guideline. A cost-effective surface planarization process was demonstrated to achieve uniform copper thickness across the panel, as well as controlling the dielectric thickness for impedance control.

Coupling enhanced electrical ring resonators were designed, fabricated, and characterized to extract the dielectric constant and loss tangent of a new photo-sensitive dry film dielectric material for defining the impedance controlled design rules based on this material. Microstrip lines and CPW lines were fabricated on glass interposers and characterized up to 20 GHz to validate the simulation results of the 3D HFSS models with the proposed process variations.

CHAPTER 1

INTRODUCTION

This dissertation presents a comprehensive analysis of the impact of re-distribution layer (RDL) processes and their variations on the electrical performance of 50 ohm impedance matched transmission lines at 2 μm critical dimensions (CD) on glass interposers for 2.5D multi-die interconnections. High performance and cloud computing as well as other emerging applications such as autonomous driving are fueling the demand for higher logic-to-memory bandwidth at lowest power consumption and lowest cost. In the past few decades, transistor scaling resulting in more transistors per unit chip area, has been the primary approach to increasing system performance while reducing cost. However, as on-chip scaling driven by Moore's law reaches performance and cost barriers, future bandwidth increases and performance improvements need system scaling at the package level [1]. There are two ways to increase the signal bandwidth and reduce the signal latency, (a) scale the bump pitch and increase the number of logic-memory interconnection channels, and (b) increase the data rate per channel. Such an architecture interconnecting multiple logic and memory devices in close proximity to each other in one package is referred to as a 2.5D interposer. Compared to traditional 2D packaging, 2.5D interposers reduce the signal interconnection length between individual devices, but more importantly, increase the number of interconnections significantly by eliminating the bottleneck of coarse pitch board-level interconnections. 3D IC stacking architecture has the shortest interconnection length and highest bandwidth possible, suitable for low power 3D memory IC stacking, but suffers from thermal and cost challenges for high

power CPU/GPU packaging [2]. Complicated cooling methods are required for the thermal management of high performance 3D stacked ICs [3-5]. The most important technology building block to enable 2.5D interposers is the design and fabrication of high density wide bus re-distribution layers (RDL) with low line resistance and capacitance, as well as precise impedance control, to scale both the channel density and data rate per channel. Much of the prior work on high density RDL for 2.5D interposers has been based on back end of line (BEOL) fabrication methods on silicon wafers, using vacuum deposited SiO_2 thin film dielectrics and copper dual-damascene processes. Such an RDL is limited in two ways in addressing the interconnect scaling roadmap needs, (a) high line resistance and capacitance due to process induced limits in copper thickness, as well as high electrical loss of silicon, and (b) low throughput process steps such as vacuum deposition of the dielectric. Georgia Tech pioneered copper-polymer RDL on glass interposers with a goal of silicon-like wiring density, but at much lower line resistance and capacitance and relatively lower cost. The electrical design of such an RDL structure is significantly different from existing BEOL design, due to the higher aspect ratio copper transmission lines and dry film polymer dielectrics instead of ultra-thin SiO_2. A recent dissertation reported on the fact that below 1 μm CDs used in BEOL RDL, RC delays are the dominant effect on the signal performance, and hence silicon interposer design guidelines have focused on RC modeling [6]. However, for the Cu-polymer RDL developed in this research, the CDs above 1 μm necessitate a design methodology based on 50 ohm impedance matching. Although a significant body of work exists for BEOL RDL design guidelines considering the impact of material property and process variations, there is a complete lack of reported literature on process variation analysis on

transmission line impedance and other electrical parameters for emerging Cu-polymer RDL on panel scale interposers. Hence, this dissertation research aims to address two major challenges in enabling 2 μm CD RDL for 2.5D glass interposer packages, namely, (1) lack of a comprehensive analysis of process variation impact on electrical performance, leading to a set of design guidelines, and (2) lack of high precision panel-scale RDL processes in controlling the transmission line dimensions to achieve 50 ohm impedance. The objective of this dissertation is to provide a comprehensive set of design guidelines for 2 μm RDL at 20-40 μm I/O pitch by modeling, design, fabrication and characterization of copper-polymer multi-layer RDL on glass interposers.

1.1 Evolution of Interposer Architecture

An interposer is an intermediate layer between ICs with fine pitch I/Os and 2D organic or ceramic BGA (ball grid array) packages connected to system board with much larger pitch sockets. The retail version of the Intel Core i7 processor is a typical example of an IC mounted on an 2D organic package with heat spreader on top (Figure 1.1). This single chip organic package includes multi-layer RDL to fan out the fine pitch interconnect at chip level to a 40 mil (1.016 mm) pitch LGA socket, as well as surface mounted discrete inductors and capacitors for signal integrity and power delivery.

Figure 1.1: Complete Package of Intel Core i7-5820K CPU

2.5D interposer architecture was inspired by the multichip module (MCM) invented back in 1980s [7], which integrated multiple smaller ICs onto a single ceramic package to compensate for the low yield of single large ICs. In the 1990s, six varieties of the MCM technology were reported, including glass-ceramic core with thin film and high density laminated RDL [8]. The first high-density 2.5D interposers in use today are based on silicon carriers with through-silicon vias (TSVs), which utilize back-end of line (BEOL) tools and processes to form multiple re-distribution layers (RDL) at ultra-fine pitch (compatible with bump pitch at 20-40 μm). Compared to organic package substrates, silicon has superior dimensional and thermal stability, as well as nanometer level surface smoothness for sub-micron wiring. Xilinx used 65nm node back end of line (BEOL) processes to demonstrate the first 2.5D silicon interposers with 45 μm interconnection bump pitch for high performance 28 Gbps FPGA systems [9, 10]. AMD applied 2.5D silicon interposer technology for their Fiji GPU with high bandwidth memory (HBM) Generation 1 mounted side by side to the logic chip, and doubled the signal bandwidth per memory die with HBM Generation 2 for VEGA GPU. The main

challenges associated with such wafer-based interposers are the high cost due to small wafer size (200-300 mm) and expensive BEOL RDL fabrication processes. Silicon interposers also suffer from high electrical signal loss due to the lower resistivity of silicon, and more importantly, high line resistances coming from the limited thickness and width of the copper traces. The third challenge with silicon interposers is the need for a BGA package to connect the silicon interposer to the board for system level reliability. Hence, organic panel interposers have been investigated as a lower cost and lower line resistance alternative with the ability to directly SMT attach to printed wiring boards. The leading edge organic interposers by Kyocera have achieved 6 μm lines and spaces wiring and 50 μm bump pitch on low coefficient of thermal expansion (CTE) organic substrates [11]. Although significant advances have been made in developing such organic interposers, they are ultimately limited in interconnect scaling due to the poor dimensional and thermal stability, as well as the non-planar surface of organic laminate cores.

Panel-based glass interposers have been demonstrated as a lower cost and higher performance alternative, to address the aforementioned challenges with organic and silicon interposers [12-14]. Glass combines the material advantages of silicon and organic laminates. The comparison of substrate materials for 2.5D interposers is shown in Table 1.1. The high modulus and tailorable CTE of glass increases its dimensional stability comparable to that of organic cores. Furthermore, its high co-planarity and low surface roughness enables fine pitch RDL trace formation. The high-resistivity of glass improves electrical performance, while the scalability to large panel processing offers potentially

lower cost compared to silicon wafers [12-15]. Figure 1.2 shows the schematic drawing of a typical 2.5D glass interposer.

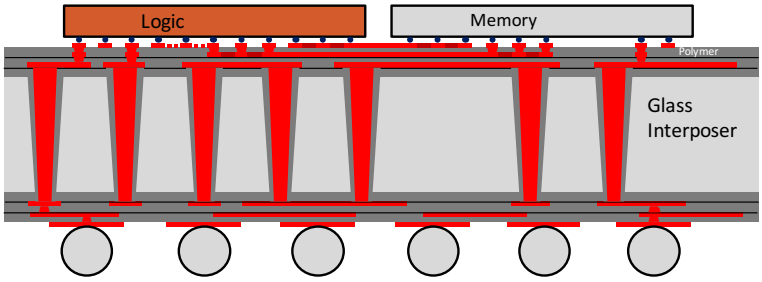


Figure 1.2: Cross-section of a typical 2.5D glass interposer (Not drawn to scale)

Table 1.1: Key electrical and mechanical properties of common 2.5D interposer substrate materials

Substrate Material	FR4	BT (Mitsubishi)	Monocrystalline Silicon	Glass
Relative dielectric constant	4.2-4.9	4.5-5.1	11.7	4-7
Loss tangent (tanδ)	0.008@3 GHz	0.006@1 MHz, 0.015 @10 GHz	0.005@1 GHz, 0.015@10 GHz	0.004@2.4 GHz, 0.006@10 GHz
CTE (ppm/K)	17	14	2.6	3-8.5
Young's Modulus (GPa)	21-24	28	130-188	50-90

1.2 Current RDL Approaches for 2.5D Interposers

The focus of this dissertation research is on the most important building block in 2.5D panel-based interposers, namely, multiple re-distribution layers (RDL) to achieve high density routing between devices at 20-40 μm I/O pitch. There are three primary methods for RDL formation used in current state of the art silicon wafer and organic panel interposers, (1) Subtractive etching process, (2) Semi-additive process (SAP) and (3) dual damascene process. Subtractive etching or semi-additive plating processes (SAP)

are used in organic interposers and package substrates. The RDL process for silicon interposers are either based on wafer level process such as dual damascene process, or the SAP method with liquid photoresist for lithographic patterning. Each RDL process approach has its own set of advantages and disadvantages. The subtractive method is the simplest and most cost-effective way to pattern copper circuits on large panels. The isotropic copper wet etch removes unwanted copper with high selectivity and is not thickness limited due to the high etch rates. However, the isotropic process etches copper both vertically and horizontally, resulting in narrower and tapered copper trace side walls, as shown in Figure 1.3. Subtractive methods are limited in aspect ratio and are not suitable for applications with critical dimension (CD) less than 20 µm.

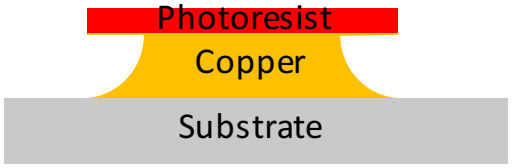
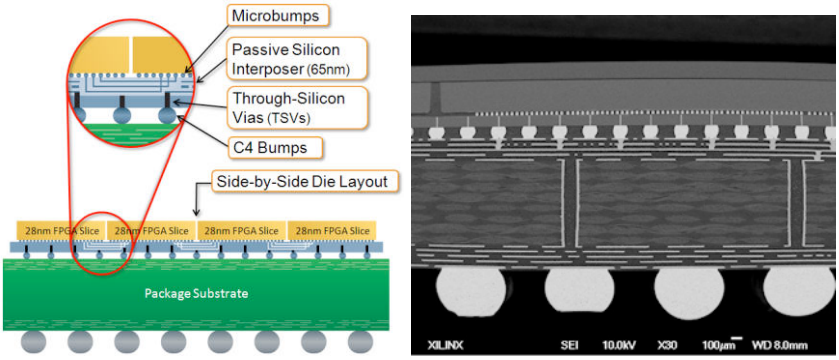


Figure 1.3: Over etch of copper trace under photoresist by subtractive method

The SAP method utilizes a thin copper layer called seed layer to form copper traces by electrolytic plating. The plated copper pattern is defined by a developed photoresist layer which transfers the designed circuit from a photo-mask to the substrate or by direct writing from a computer controlled imaging tool. After the copper metallization, the thin seed layer needs to be removed by a copper etchant. Since the seed layer is much thinner (typically 200-300 nm) than the metallized copper traces, the etch time is much shorter than subtractive copper etching. The copper trace side wall etch amount is roughly the copper seed layer thickness, making this method suitable for

circuits with CDs less than 20 µm. With high resolution photolithography processes on silicon wafers and optimized copper seed layer etch processes with end point detection, the SAP method has been demonstrated down to 1.6 µm pitch routing on silicon interposers, although the limited metal thickness would lead to undesirable, high electrical resistance [16].

Traditional silicon interposers utilize wafer level BEOL processes to fabricate sub-micron routing traces, as shown in Figure 1.4. The most common dual damascene process etches the via and trace layer patterns into ultra-thin silicon oxide dielectric films by deep reactive ion etching (DRIE), followed by sputtering of Ti-Cu seed layers into the trenches and vias, and electroplating to fill the trenches and vias, and finally a chemical mechanical polish (CMP) step to remove the copper overburden on the surface to form the RDL layers. Since this process eliminates the need to etch copper, it results in highly precise CD control down to sub-micron lines and spaces. However, the high line resistance caused by the ultra-thin and narrow copper trace limits the line lengths for chip-to-chip interconnections.



(a) (b)

Figure 1.4: (a) Schematic cross-section view of Xilinx's silicon interposer technology, and (b) The SEM cross-sectional image of the 28-nm Xilinx's Virtex-7 device [9]

1.3 Limitations of Current RDL Approaches

As shown in Figure 1.5, there is an interconnect gap or RDL gap between the current organic substrates which are limited to 5-8 μm lines and spaces, and wafer BEOL silicon interposers, which have less than 1 μm lines and spaces fabricated with expensive wafer level tools. Furthermore, signal routing with BEOL technology has high line resistance and capacitance, due to the small cross-sectional area of lines and ultra-thin silicon dioxide dielectric layers. High resistance and capacitance leads to high RC delay for signal transmission, degrading interconnect performance, and limiting interconnect length. Organic interposers with wider routing wires have much lower signal latency, but at the cost of routing density. RDL scaling on organic laminate substrates below 8-10 μm CDs faces fundamental challenges due to the non-planarity of the polymer-glass composite material, as well as warpage during the curing of additional polymer interlayer dielectrics. High resolution lithography tools used to image circuit patterns typically have a depth of field of less than 10 μm for high yield and uniformity of line widths across large wafers or panels. The non-planarity of laminate substrates is in the 3-5 μm range, and warpage can significantly exceed the depth of focus limits, thus causing yield loss during lithography. An additional design requirement for low latency RDL traces is the high degree of impedance control that is required as the signal data rates in individual channels extend into the multi-Gbps regime. The RDL on glass interposers demonstrated in this dissertation research aims to address this RDL gap by overcoming the fundamental design and process challenges in achieving high density multilayer RDL with low line resistance and capacitance, as well as precise 50 ohm impedance matching on panel-based interposers using dry film polymer materials.

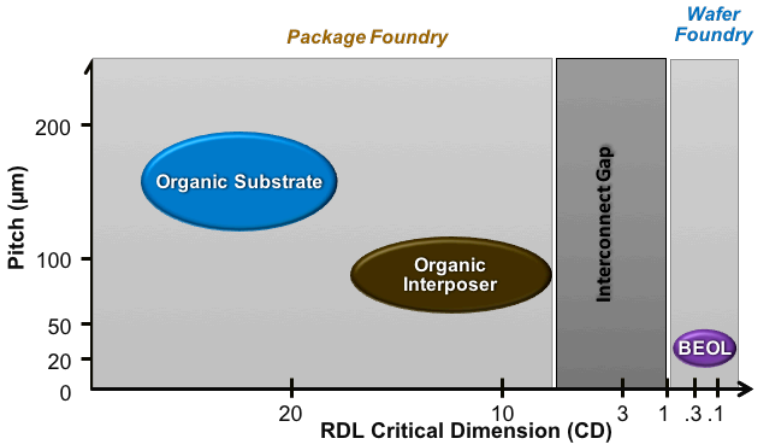


Figure 1.5: Current Technologies with different bump pitch and RDL CD

1.4 Novelty of Dissertation Research

Glass was chosen as the core material for ultra-fine pitch multi-layer RDL fabrication, primarily due to its unique combination of ultra-thin panel availability, smooth and flat surface, and exceptional dimensional stability. The ultra-smooth glass surface results from draw processing used to form thin sheets with a typical average roughness (R_a) less than 10 nm, and total thickness variation (TTV) in the single digit micron range across a 500 mm x 500 mm panel area. This lends itself well to scaling fine line RDL below 5 µm with high yield lithography processes, the same reason silicon has been the material of choice for scaling on-chip wiring. Although silicon wafers also offer such a smooth and flat surface for RDL formation, they need to be polished to achieve the substrate thickness and surface smoothness targets, resulting in higher cost. RDL processing on silicon wafers is single sided, and the RDL on glass process is double-sided, providing back side routing layers at no added cost to fan-out to large pitch for direct SMT attach to PWB. The body size of 2.5D interposer packages is also expected to scale to 40 mm x 40 mm and larger to accommodate multi-die integration, and this results

in a limited number of interposers on one silicon wafer. This research proposes and demonstrates a dry film polymer based large panel scalable RDL formation method with low line resistance and capacitance for 2.5D panel-based interposers by overcoming several fundamental process challenges, and quantifying the impact of process variations on controlled impedance transmission lines, leading to 2 µm lines and spaces at 20 µm I/O pitch, impedance controlled RDL design guidelines for the first time. The key innovations in this research are shown in Figure 1.6, namely, (1) the first comprehensive modeling and design analysis of 2 µm transmission lines at 20 µm I/O pitch to quantify the effect of process variations, and (2) process control enhancements to achieve highly controlled 50 ohm impedance transmission lines at 2 µm widths and spacing, both on panel-scalable glass interposers.

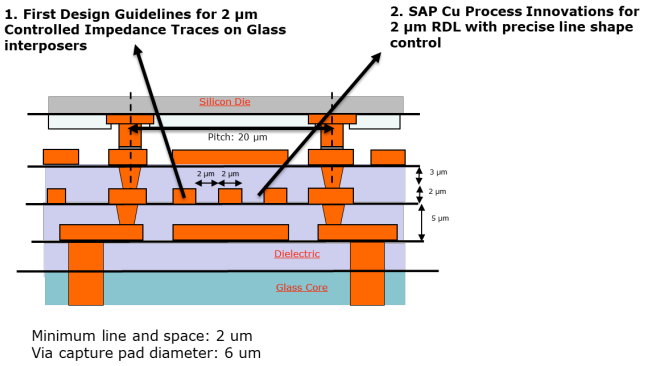


Figure 1.6: Novelty of Dissertation Research in RDL on Glass Interposers

1.5 Research Objectives and Challenges

The objective of the proposed research is to model, design and demonstrate impedance-matched 2 µm multilayer RDL lines and spaces for 2.5D panel-based interposers, compatible with 20 µm bump pitch, with glass as the core material. The fundamental studies in this research focus on exploring several unit process methods to

address the process challenges, and systematically analyze the signal performance impact due to process variations using 3D electro-magnetic simulations, leading to impedance controlled RDL design and fabrication guidelines. This dissertation represents the first systematic design and demonstration study of 50- ohm controlled impedance, 2 µm CD transmission lines on glass interposers.

Figure 1.7 illustrates the two major fundamental technical challenges addressed in this research. Table 1.2 lists the specific technical objectives compared with prior art and fundamental challenges in achieving the goals of this research.

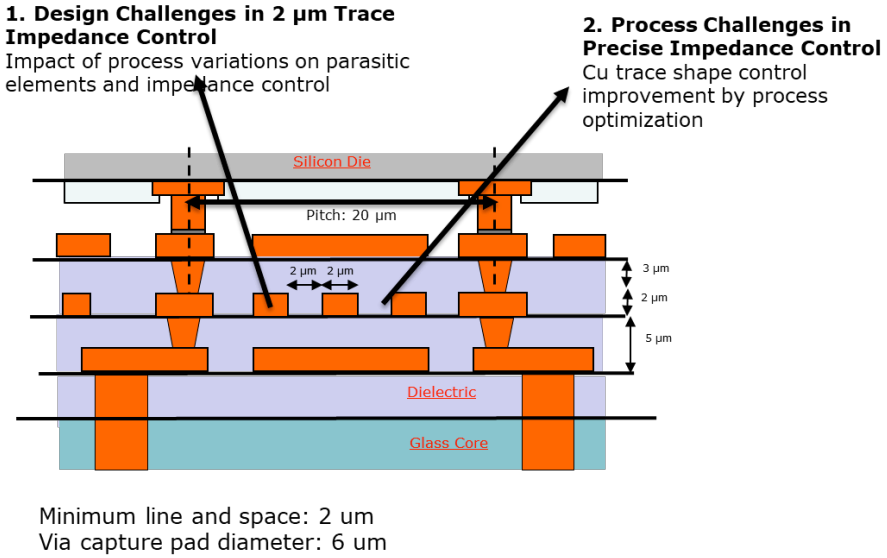


Figure 1.7: Schematic view of impedance matched 2 µm CD RDL with challenges

Table 1.2: Research objectives and challenges

Parameters	Objective	Prior Art	Challenges
Impedance control	50-ohm impedance multilayer RDL at 2 µm lines with impedance tolerance up to 10%	50-ohm design rules at line widths > 6 um, no process impact studies reported	Interaction of multiple process-induced variations in line geometries
Wireability for 20 µm bump pitch	200 lines/mm for one routing layer (6 µm capture pad with 2 µm line and space)	40 lines/mm at 50 µm bump pitch for typical organic interposer	Limitations of the SAP method

SAP was selected as the front-up method for multilayer RDL fabrication on glass interposers, mainly due to its scalability to both wafers and panels, and its compatibility with high throughput manufacturing. The emerging embedded trace method inspired from wafer level dual-damascene processes was also analyzed by electromagnetic simulations. To achieve the wiring density goal with impedance control, two main research challenges were identified:

(a) Lack of a comprehensive analysis of the fabrication process variation impact on the electrical performance of the impedance controlled RDL traces to define process tolerances for the specified impedance targets.

(b) Lack of high precision panel-scale RDL fabrication processes in controlling the transmission line dimensions to achieve 50 ohm impedance target at 2 μm lines and spaces.

1.6 Research Tasks and Proposal Organization

To address these process challenges and analyze the impact of process variations on the signal performance, two fundamental research tasks and one demonstration task are proposed: (1) modeling and design of impedance controlled RDL to quantify the process variation impact, (2) ultra-fine and high precision RDL fabrication process research to improve RDL precision, and (3) electrical characterization of RDL materials and transmission lines, leading to the demonstration of impedance controlled fine line RDL. This dissertation is organized into the following chapters.

Chapter 1 describes the background and strategic need for this work. The research objectives are proposed and the technical challenges as well as research tasks are identified to achieve these objectives.

Chapter 2 summarizes the prior art on RDL design and fabrication on organic, silicon, and glass interposers.

Chapter 3 describes the impedance controlled transmission line design for glass interposers with leading edge dry film polymer dielectric materials, and simulations of performance impact due to process variations for both SAP and embedded methods. Four critical process variations were chosen to study the electrical performance impact of different transmission lines on the package. These are: (1) narrower copper traces, (2) tapered copper traces, (3) thicker or thinner copper traces, and (4) conductor surface roughness. The process impact on RLCG elements of the transmission lines as well as the impedance were analyzed. The performance sensitivity of the four major process variations were identified, resulting in a complete set of process design guidelines.

Chapter 4 summarizes SAP process advances in overcoming the following major process challenges: (1) high resolution panel compatible lithography with dry-film photoresist materials, (2) high yield and high quality electrolytic copper plating using a new high throughput ozone cleaning process, (3) advanced copper seed layer etch processes with significant reduction in copper trace damage, and (4) surface planarization to improve thickness uniformity for multi-layer fabrication and better impedance control.

Chapter 5 discusses the characterization of the fabricated fine transmission lines, and the design and characterization of an enhanced coupling ring resonator test structure for a new photo sensitive dielectric material to scale the layer to layer via interconnections to the same dimensions as the lines.

Chapter 6 summarizes the key findings and scientific contributions of this dissertation, and identifies the future work in this research topic.

CHAPTER 2

LITERATURE SURVEY

CHAPTER 1 introduced the objectives of this research, and the dissertation research tasks on the electrical design and simulation, process advances, and electrical characterization of the multi-layer RDL, a key building block in 2.5D interposers. The fundamental challenges identified to achieve the objectives are: 1) the accuracy of impedance control due to various fabrication process related issues and 2) high aspect ratio double side panel compatible fabrication challenges with dry-film technology. This chapter provides a comprehensive review of the published literature in addressing these technical challenges organized into impedance controlled design, low resistance wiring, and high density RDL process demonstration on various substrates.

2.1 Prior Art on Impedance Controlled Design and Process Impact

This section provides a brief overview of selected publications on design rules for target impedance, and fabrication process impact on impedance control. For high performance digital applications, when the signal flight time (delay) of the interconnect is longer than the signal bit period, two bits of signals or more co-exist on one interconnection channel. If the interconnection channel has any impedance mismatch, echoes of the previous pulse can blend into the current pulse and corrupt it, causing signal integrity issues. The common method to mitigate this issue is to control the impedance across the entire interconnection channel. In the interposer package design, the most commonly used characteristic impedance for single-ended channels is 50 ohms.

In 2014, Kyocera [11] introduced the Advanced Package X (APX), an advanced organic substrate process for 2.5D interposers. The major features were fine pitch wiring with impedance match to support 2.5D interposer signaling, power plane pattern compatibility, lower insertion loss compared to silicon interposers, high stiffness, and low-cost potential. Impedance controlled design rules were provided for the APX RDL, as shown in Figure 2.1. Although the claimed minimum wiring line and space was 6 µm, the impedance controlled minimum line width was 7.5 µm for the strip line, due to the lack of ultra-thin dielectric materials.

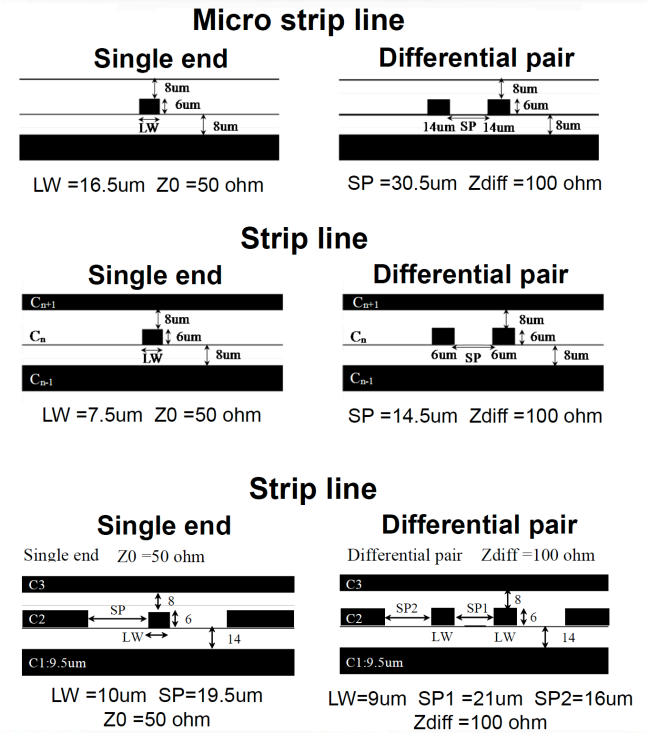


Figure 2.1: Design rule for impedance control by APX [11]

Ka Fai Chang et al. from A*STAR [17] reported impedance controlled transmission line performance on silicon interposers. Microstrip lines, coplanar

waveguide (CPW), grounded CPW, and differential CPW were designed with impedance matching on build-up layers on the silicon substrate. Without ground shielding, the electromagnetic field will penetrate through the polymer into the silicon substrate. Therefore, by using high resistivity silicon substrate, the insertion loss of CPW can be significantly reduced, especially above 10 GHz frequency, as shown in Figure 2.2. All four types of designed transmission lines were fabricated and measured. The microstrip line, CPW, and differential CPW showed 0.3 dB/mm, 0.35 dB/mm, and 0.32 dB/mm insertion loss up to 40 GHz respectively, while the grounded CPW showed much higher insertion loss (0.56 dB/mm) due to the radiation loss at the resonant frequencies. The results also conclude that the substrate loss for CPW is not significant.

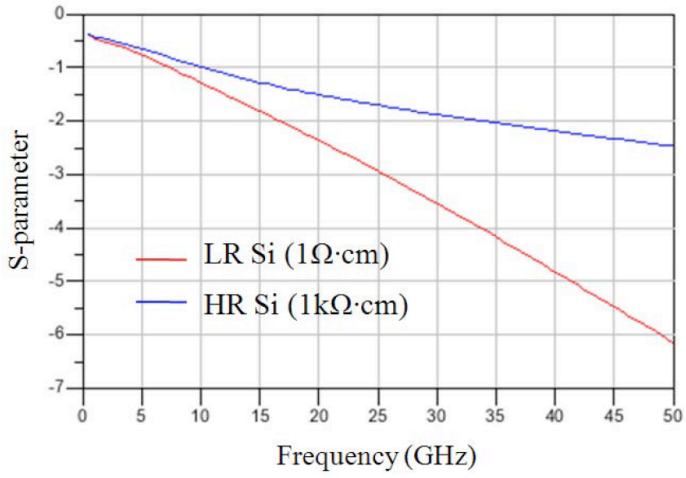


Figure 2.2: Simulated insertion loss of CPW with different silicon substrate resistivity [17]

Abdelghani Renbi et al. from Luleå University of Technology [18] presented the etch process impact on the transmission line characteristic impedance and crosstalk on

high density interconnect boards. Three copper trace side wall angles were considered, as shown in Figure 2.3. Four impedance matched copper traces with different width (200 µm, 150 µm, 100 µm, and 50 µm) and same copper thickness (18 µm) were analyzed. With tapered side walls, the effective copper trace width is reduced, leading to impedance increases of up to 10%. However, reducing the copper trace width increases the space between traces, which results in crosstalk reduction. With the same routing density, the impedance error can be traded for lower crosstalk for applications which place a high priority on crosstalk reduction.

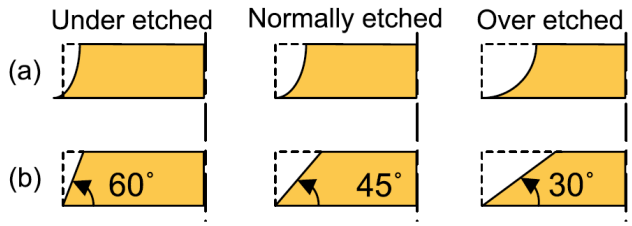


Figure 2.3: Copper side wall shape after etch process: (a) etch shapes, (b) equivalent shapes [18]

There is a complete lack of prior art in impedance controlled design and process variation impacts for fine lines below 5 microns, mainly due to the lack of ultra-thin dielectric materials and scaling challenges of existing package substrate RDL processes.

2.2 Prior Art on High Density RDL Demonstration

2.2.1 RDL with High Aspect Ratio for Low Resistance

This section provides a brief overview of selected publications on high aspect ratio RDL patterning and metallization. Reducing copper trace resistance and capacitance

reduces the signal delay and cross talk, resulting in improved signal integrity. The common method to reduce trace capacitance involves the use of low-K dielectric materials or even air-gaps [19] between interconnection paths. At certain aspect ratios, the copper trace resistance per unit length is proportional to the square of the routing density. Higher routing density leads to much higher line resistance, which will eventually cause signal integrity issues. One simple way to reduce the trace resistance while maintaining the routing density is to increase the aspect ratio of the trace. In 2009, Shinko [16] demonstrated multilayer RDL on silicon substrates with SiO_2 as the insulation layer by the SAP method, and also explored high thickness copper wiring for low resistance. Copper traces with 8.75 µm thickness and 2.4 µm width were fabricated on the silicon interposer, as shown in Figure 2.4. However, the copper trace resistance and copper seed layer etching technique were not reported in this paper.

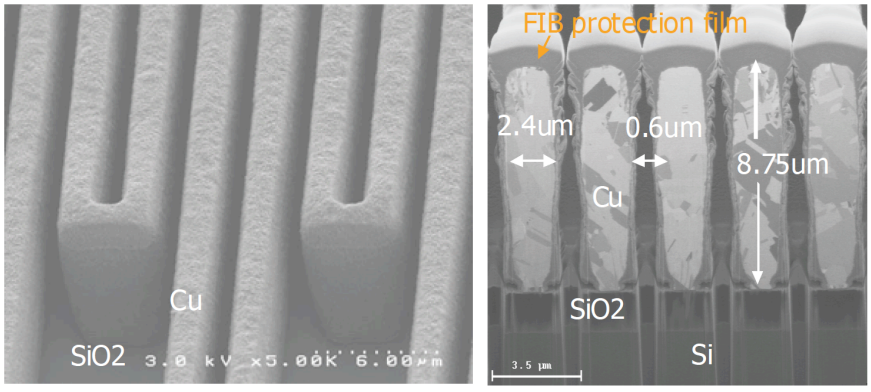


Figure 2.4: High thickness fine Cu wiring at pitch of 3 µm [16]

To achieve high aspect ratio copper wiring with the SAP method, high resolution negative tone resist materials were described by Hisanori Akimaru, et al. [20] A new negative tone resist was formulated by combining different photo initiators and polymers

to achieve less than 2 μm resolution and larger than 3 aspect-ratio. Copper traces with 2.5 μm thickness were metallized by electrolytic plating on sputtered copper seed layers on silicon wafers with patterned photoresist layers, as shown in Figure 2.5. This work did not show the trace profiles after seed layer etch, and utilized liquid photoresists, which limit its applicability to panel processing.

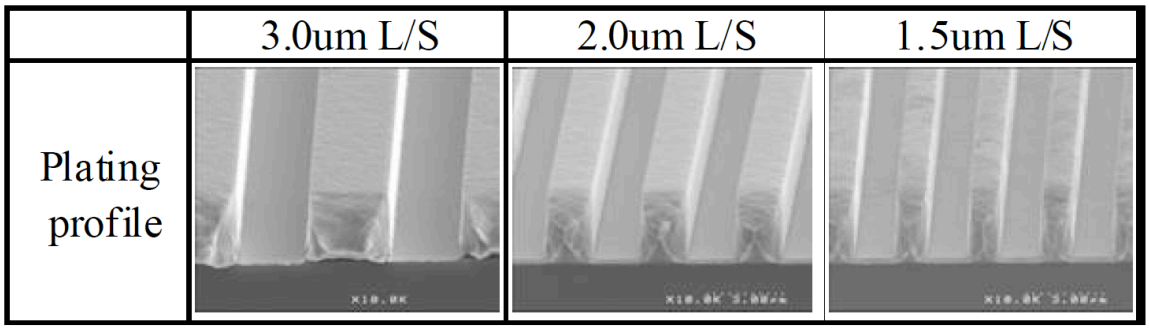


Figure 2.5: SEM images of metallized copper traces on seed layer [20]

Lithography tools with depth of focus (DOF) that is larger than the photoresist thickness is a prerequisite for high aspect ratio RDL patterning. Keith Best et al from Rudolph Technologies [21] demonstrated a lithography process for 2 μm resolution patterns in 10 μm thick photoresist, as shown in Figure 2.6. The type of photoresist used (dry-film or liquid) was not reported.

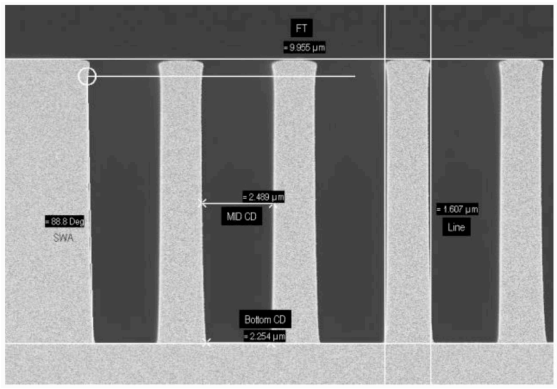


Figure 2.6: SEM cross section of 2 µm width copper walls with 10 µm thickness [21]

Although several publications reported on high aspect ratio lithography with liquid photoresist, there has been limited progress in high aspect ratio RDL lithography processes for low resistance with dry-film resist materials. A bigger and unaddressed challenge is the deposition of ultra-thin dry-film polymer dielectrics to achieve precise impedance control, low overall interconnect signal delay and high routing density.

2.2.2 Semi-Additive Process for RDL Wiring

This section provides a brief overview of RDL wiring formation on various substrates with package level and wafer level processes. The latest organic interposers use low CTE and high modulus polymer-glass composite materials as the core substrate. The RDL layers on top and bottom are balanced in a mechanically symmetric structure to minimize warpage during fabrication. Kimihiro et al. [22] demonstrated fine patterning of 8 µm line width and spacing with 100 µm via pitch on a low CTE (3 ppm/°C) organic substrate called Advanced Surface Laminar Circuit (Adv-SLC), as shown in Figure 2.7. The CTE of the laminate core could be tailored by a small amount by adjusting the volume ratio of the resin in the core. Both through package vias and micro-vias were formed by 266 nm UV YAG laser ablation. The RDL was formed by a standard SAP with sputtered NiCr and Cu seed layers. The build-up dielectric film had a CTE close to 0

ppm/°C, which also contributes to the low CTE of the entire package. The authors stated that the flatness of the underlying dielectric surface was essential for achieving fine line and space wiring, whereas copper surface roughness improved the adhesion to the surrounding dielectric materials. The eye-diagram of the longest chip-to-chip signal path was simulated, showing that the small test chip with short interconnection lengths (23 mm) had an acceptable opening eye at 20 GHz, while the large test chip with longer signal path (98 mm) had a closed eye even at 10 GHz.

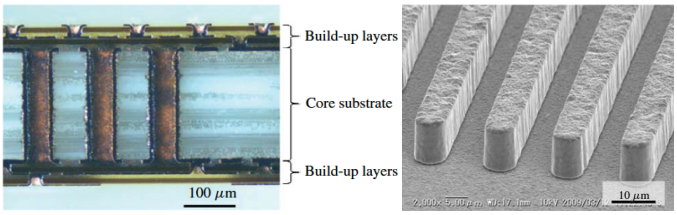


Figure 2.7: Multi-layer RDL on organic core with 8 μm in line width and spacing [22]

Kyocera reported on processes used to form RDL in the Advanced Package X (APX) [11], where the minimum wiring line and space was improved from 8 μm to 6 μm, and the maximum stack-up layer count was 5-2-5, larger than the Adv-SLC layer stack-up of 4-0-4. The simulation results showed that the APX had much lower loop inductance and smaller backward cross talk noise compared to the current organic substrates due to the thinner core of APX.

Masahiro et al. at Shinko Electric Industries Co., Ltd reported on the fabrication processes for silicon interposers with Cu-TSVs in 2008 [23], and an improved version in 2009 [16]. The multilayer RDL was formed by an advanced SAP method. However, wafer based tools and processes to form Cu-polymer RDL were applied to achieve 1.6 μm pitch wiring. Since CMP was not used between layers, the wiring surface was not flat for the second and subsequent layers. Furthermore, due to the seed layer etching step, the

width of the copper wiring was 0.43 µm, much smaller than the target width of 0.8 µm, as shown in Figure 2.8. However, the electrical performance of RDL was not reported in this paper.

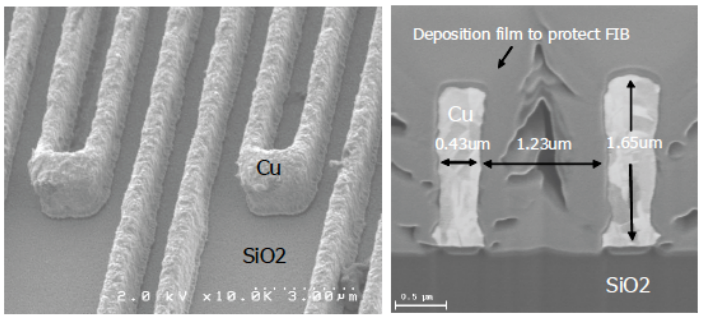


Figure 2.8: Copper traces on SiO2 at 1.6 µm pitch [16]

A similar process was demonstrated on organic interposers by Kiyoshi Oi et al from Shinko Electric Industries Co., Ltd [24] in 2014. Photo-sensitive dielectrics were utilized for multilayer RDL fabrication, and a CMP process was employed to expose the first metal layer on the conventional substrate. This polishing step adds a significant amount of cost and complexity to the interposer fabrication process. This high density organic package had a total of eight metal layers with a first level interconnection bump pitch of 40 µm, as shown in Figure 2.9.

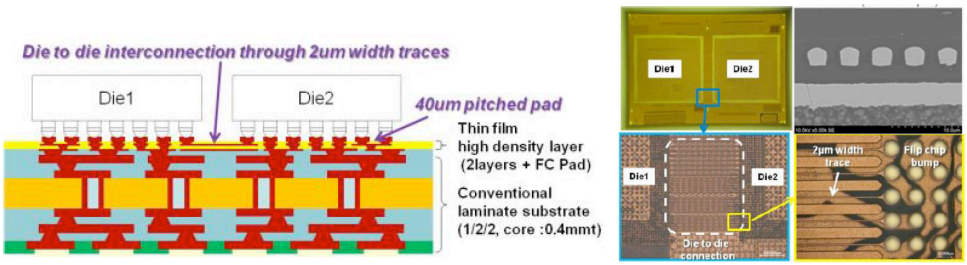


Figure 2.9: Schematic cross section of organic interposer and 2/2 µm line and space demonstration on organic interposer with photo vias [24]

Christian Romero et al. from Samsung Electromechanics Co, Ltd [25] demonstrated an organic interposer with line and space below 5 µm and micro-via pitch below 50 µm (Figure 2.10). The standard SAP method was used for trace metallization, with photo-sensitive dielectric layers for micro-via formation. The minimum line and space demonstrated was 3 µm, a comb structure for open/short reliability testing. All the samples passed the B-HAST test for 96 hours, with no significant deviation of the resistance values as compared to 0-hour readings. The measured insertion loss of 3 µm line with 5 mm length was about -0.2 dB at 1 GHz and -0.3 dB at 2 GHz.

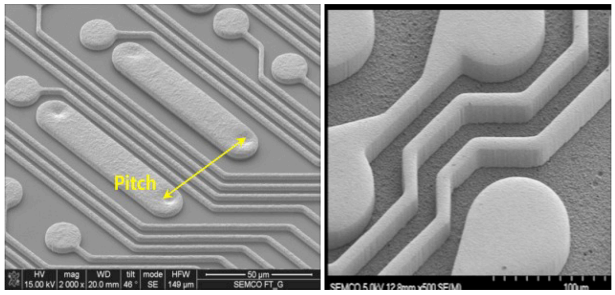


Figure 2.10: SEM image of die-to-die interconnects and escape routing lines at pitch below 50 µm [25]

The SAP method has been extended to glass substrates. Chun-Hsien Chien et al. at Industrial Technology Research Institute (ITRI) in partnership with Corning Incorporated demonstrated glass wafer interposers for 3D integration as shown in Figure 2.11 [26]. The first copper layer was directly metallized on the glass substrate using the SAP method with sputtered Ti/Cu seed layers. The width and the thickness of the demonstrated copper traces were 40 µm and 6 µm, respectively. Zhiming Liu et al at Atotech USA, Inc. [27] demonstrated a thin metal oxide adhesion promotion layer called VitroCoat^{TM} layer on glass substrates for improved copper-to-glass bonding. The

Through-Package Via (TPV) metallization and RDL formation used the SAP method with electroless deposited copper seed layers instead of sputtering.

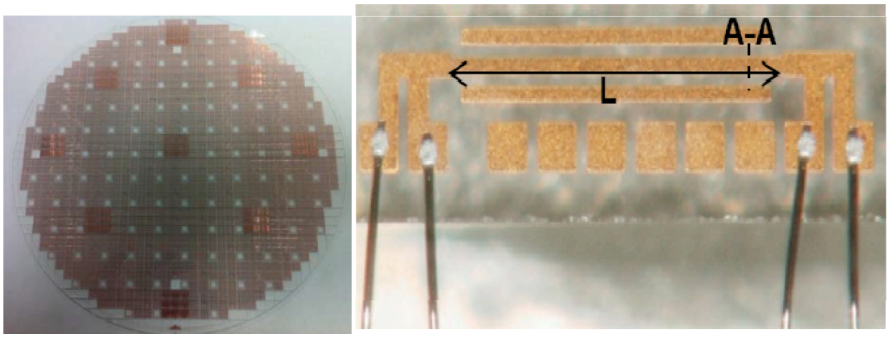


Figure 2.11: Glass wafer test vehicle (left) and reliability evaluation pattern (right) [27]

2.2.3 RDL Processed by Embedded Method

Inspired by the wafer level damascene process, the embedded trench method was explored for Cu-polymer RDL, due to the elimination of the seed layer etching step one of the factors limiting the RDL scaling of the SAP method. The major difference between this approach and the damascene process used for silicon wafers, is the use of either lithography process on photo-sensitive dielectric materials or laser ablation in non-photosensitive polymer dielectric materials to form trenches, in lieu of deep reactive ion etching of silicon oxide thin film dielectrics in the wafer damascene process. At the Georgia Tech Packaging Research Center, trenches as small as 1.5 μm widths and spacing were formed in the liquid photo-sensitive layer PN-0371D on polymer laminated glass substrates. [28] The cross section of metallized fine line traces from 1.5 μm to 5 μm are shown in Figure 2.12 with copper thickness of 4 μm. Photo-sensitive dry film with 10 μm thickness was also tested, showing 3 μm resolution.

Figure 2.12: Cross section of embedded 1.5 to 5 µm L/S in PN-0371D photo-sensitive material on polymer laminated glass substrate [28]

Dyi-Chung Hu et al from Unimicron Technology Corp. [29] demonstrated a 2 µm embedded fine line process on organic interposers. The trench for fine copper wires were formed in a photo-sensitive polymer layer, while the vias were laser ablated in the ABF layer. Emulating the dual damascene process flow, both vias and trenches were filled by seed layer deposition and copper plating at the same time, and the copper overburden was removed by CMP. The process flow is shown in Figure 2.13, and the cross-sectional views of 2 µm routing with 30 µm vias are shown in Figure 2.14. The cross-sectional shape of copper traces was an upside-down trapezoid, and the electrical properties of the photo-sensitive dielectric was not reported.

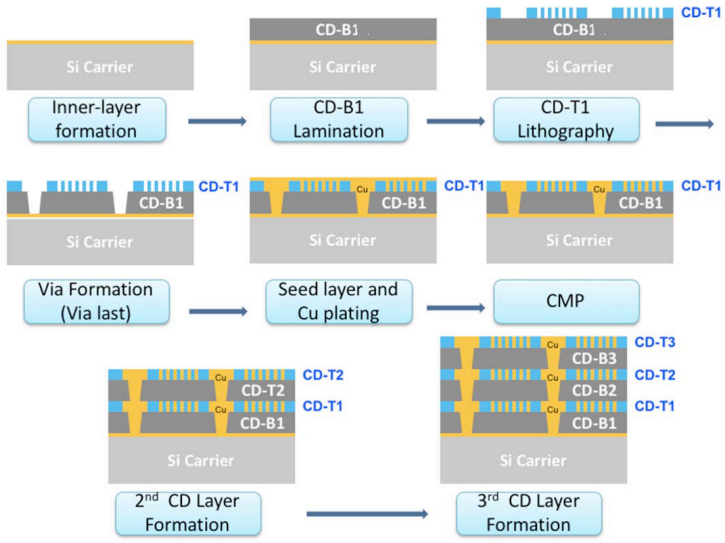


Figure 2.13: Process flow of the three-layer fine line embedded trace technology [29]

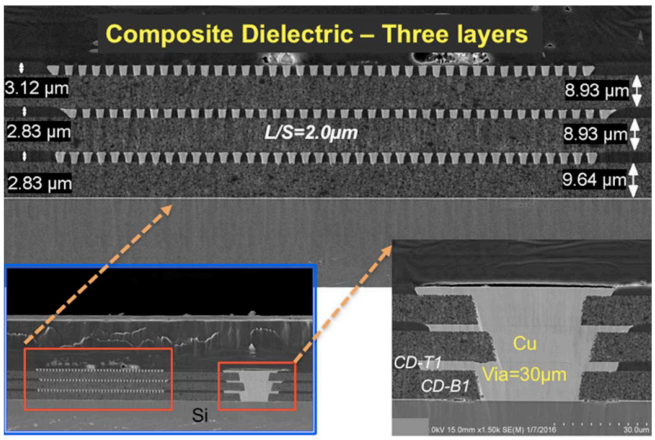


Figure 2.14: Cross section of the three-layer embedded trace demonstration with 2 µm L/S and 30 µm vias [29]

2.2.4 Back-End-of-Line (BEOL) RDL Processes

The copper wiring and vias on IC chips are fabricated by a dual damascene process. This mature BEOL wiring process was adopted to fabricate silicon interposers to provide the highest wiring density, achieving up to 10,000 die-to-die interconnections with less than 1 µm line and space routing. The first example of silicon interposers is the Xilinx FPGA interposer [9, 10], which utilized mature 65 nm node BEOL processes with high-yield in 2011, as shown in Figure 2.15. Around mid-2015, the first high-volume product, AMD's Fury computer graphic card [30, 31], utilizing 2.5D silicon interposers to integrate the HBM with GPU was introduced. Four DRAM dies and one logic controller die at the bottom of the chip stack formed one HBM die with Through-Silicon Vias (TSVs) and microbump interconnects. The HBM die had a 1024-bit bus width and operated at a clock speed of 500 MHz, equivalent to 1 Gbps. Each interposer package included one GPU die and 4 HBM dies, forming a total memory bus width of 4096-bits. The HBM with interposer provided 60% more bandwidth and 60% lower power

consumption than GDDR5, and the PCB area occupied was reduced by 3X. The SEM cross section image of the AMD Radeon™ Fury GPU is shown in Figure 2.16.

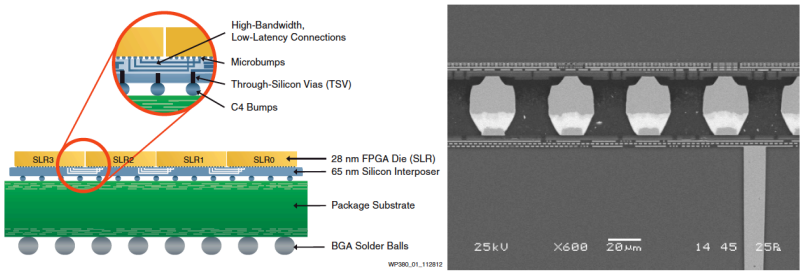


Figure 2.15: Schematic view of Xilinx's silicon interposer (left) and SEM cross section of fine line RDL with micro-bumps at first level interconnect (right) [9, 10]

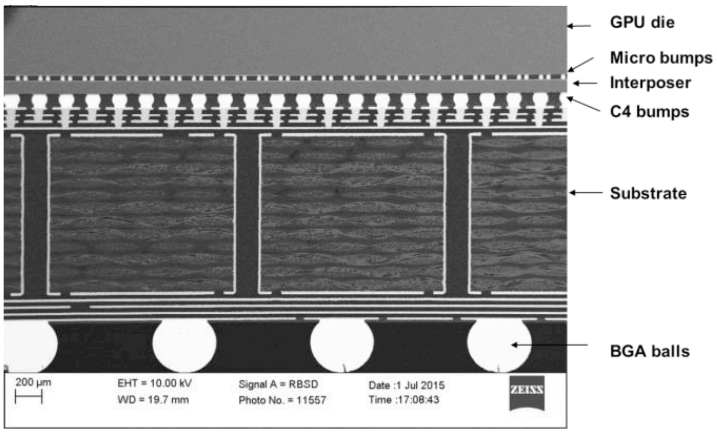


Figure 2.16: SEM image of micro structure of AMD Radeon™ Fury GPU [31]

The main challenges associated with wafer-based silicon interposers are the high resistance of ultra-thin copper traces, and high cost due to small wafer size, RDL fabrication cost, and the cost of through-silicon-vias (TSVs). Intel [32] reported on the embedded multi-die interconnect bridge (EMIB) approach in 2015. The EMIB uses a very small silicon die with multilayer RDL fabricated by BEOL processes. This small die was embedded in an organic substrate, providing silicon-like very high density chip-to-

chip interconnections without the use of a large silicon interposer and eliminating the TSVs, as shown in Figure 2.17. The die assembly to the package was based on the standard flip chip assembly process. This innovative approach required chip and package co-design to ensure all the fast channels were on the edge of the chip to form interconnections with EMIB, and the reliability due to CTE mismatch between silicon bridge and organic substrate remains unknown.

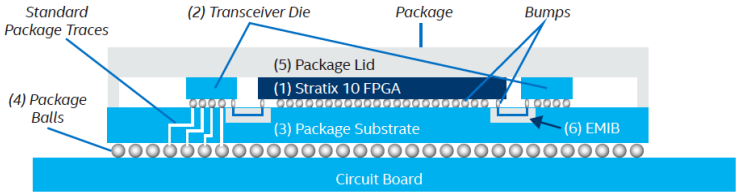


Figure 2.17: Schematic cross section of the whole multi-chip assembly with EMIB [32]

In summary, although several publications have demonstrated various RDL scaling from high cost wafer level processes to low cost package level processes, there is still a need to develop panel-compatible processes with precise impedance control, silicon-like RDL wiring density, but with lower resistance and capacitance and low cost comparable to organic substrates. There is also a lack of a complete set of design rules for Cu-polymer RDL including the effects of various process variations, to enable future glass interposer designs.

CHAPTER 3

CHARACTERISTIC IMPEDANCE CONTROLLED FINE LINE RDL DESIGN AND SIMULATION

This chapter presents the characteristic impedance controlled RDL design based on advanced RDL materials and processes, as well as the analysis of fabrication process variation impact on the interconnect electrical performance. The impedance matched design rules for microstrip, stripline, and Co-Planar Waveguide (CPW) transmission lines were confirmed by the Ansoft 2D extractor model. Four critical process variations are chosen to study the electrical performance impact of different transmission lines on the package. These are: (1) copper trace width, (2) copper trace taper, (3) copper trace thickness, and (4) conductor surface roughness. The resistance (R), inductance (L), capacitance (C), conductance (G), and impedance variation were calculated from the 2D extractor model. The impedance sensitivity of all four process variations were analyzed to determine the most critical process control for each type of transmission lines.

3.1 Impedance Controlled Design of RDL Transmission Lines

The RDL on an interposer consists of transmission lines for horizontal connection and small vias for vertical connection. This section describes the research on impedance controlled transmission line designs based on advanced RDL materials and processes on glass interposers.

For high-performance digital applications, when the signal flight time (delay) of the interconnect is longer than the signal bit period, two bits of signals or more co-exist on one interconnection channel. If the interconnection channel has an impedance

mismatch anywhere, the echoes of the previous pulse can blend into the current pulse and corrupt it, causing signal integrity issues. This echo only occurs in the presence of an impedance discontinuity. A good impedance match also minimizes the reflected power by equalizing the load impedance to the source impedance. The common method to improve the signal integrity is to match the impedance across the entire interconnection channel. In the package, the typical characteristic impedance of single-ended channels is set to 50 ohms. Three common types of transmission lines, microstrip line, stripline, and CPW, were designed for the impedance match at 50 ohms on a glass interposer. Ajinomoto Build-up Film (ABF) was selected as the dielectric material for the glass interposer, for its high adhesion strength with low surface roughness, low warpage during cure and reflow, high insulation reliability, and compatibility with electroless copper seed layer plating process. The specific ABF types utilized in the design were GX-92 and GX-92P, with three different thicknesses of 5 μm, 10 μm, and 15 μm. The resin formulations of these two dielectrics are identical. The major difference is the thickness availability, where GX-92P is 5 μm thick and GX-92 is available in multiple thicknesses above 10 μm. For both types, the material relative dielectric constant is 3.2 and the loss tangent is 0.017, measured at 5.8 GHz. The design rule to achieve 2 μm width and 2 μm thick impedance controlled copper trace was extracted with the ultra-thin dielectric material requirement, setting the future target for the material properties. The targeted process for multilayer RDL fabrication was an advanced SAP method which will be discussed in detail in the next chapter, as well as the emerging embedded trace method which was developed as an alternative for RDL scaling as SAP reaches its limit. For the SAP method, the dry film polymer for build-up layer is deposited with pressure on the

fabricated copper patterns during lamination. The vertical distance between the two copper layers is smaller than the original dry film thickness. On the other hand, the copper traces fabricated by the embedded trace method are buried within the surface of the dielectric layer. Therefore, the effective polymer thickness for both methods are different, as discussed in detail in the following sub-sections.

3.1.1 Microstrip Line Design

As shown in Figure 3.1, the signal path and return path for microstrip line are on different metal layers. With the SAP method, the polymer is pressed onto the metal layer under high pressure during lamination process, resulting in a reduced effective polymer thickness. In the case of the embedded trace method, the entire signal trace is embedded into the polymer. To simplify the calculation for both cases, the effective polymer thickness is assumed to be the original polymer thickness minus the copper thickness. When the signal passes through the microstrip line, part of the electromagnetic (EM) field exists in air, causing the effective dielectric constant ε_e to be less than the substrate's dielectric constant. To calculate the impedance of a microstrip line, the ε_e needs to be calculated first, by the following equations,

$$\begin{cases} \varepsilon_e = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left[\left(1+12\left(\frac{H}{W}\right)\right)^{-\frac{1}{2}} + 0.04\left(1-\left(\frac{W}{H}\right)\right)^2\right] & when\ \left(\frac{W}{H}\right) < 1 \\ \varepsilon_e = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+12\left(\frac{H}{W}\right)\right)^{-\frac{1}{2}} & when\ \left(\frac{W}{H}\right) \geq 1 \end{cases} \tag{3.1}$$

where W is the width of microstrip line, H is the effective dielectric thickness, and ε_r is the polymer relative dielectric constant. With the obtained effective dielectric constant, the characteristic impedance Z_0 in ohms can be calculated by:

$$\begin{cases} Z_0 = \frac{60}{\sqrt{\varepsilon_e}} ln\left(\frac{8H}{W} + \frac{W}{4H}\right) & when\ \left(\frac{W}{H}\right) < 1 \\ Z_0 = \frac{120\pi}{\sqrt{\varepsilon_e} \times \left[\frac{W}{H} + 1.393 + \frac{2}{3} ln\left(\frac{W}{H} + 1.444\right)\right]} & when\ \left(\frac{W}{H}\right) \geq 1 \end{cases} \quad (3.2)$$

These equations are approximate, and the copper strip thickness and whether the strip is embedded or not are not taken into account. The 2D extractor model gives the more accurate impedance at the cost of calculation time if the accuracy is required, and the model is compatible with any fabrication method. Table 1.1 shows the impedance controlled microstrip line trace width calculated by 2D extractor at 5.8 GHz. In the 2D extractor models, the solution frequency was set at 30 GHz, and the percentage errors of both admittance and impedance were set at 0.1%. The characteristic impedance is a function of frequency, and therefore, a frequency sweep was added to the solution from 0.5 GHz to 30 GHz, in 0.5 GHz steps. The solve options for both signal and ground metals were set to "solve inside". According to the simulation, the microstrip line by the embedded method has a narrower trace width with the same effective dielectric thickness due to higher effective dielectric constant.

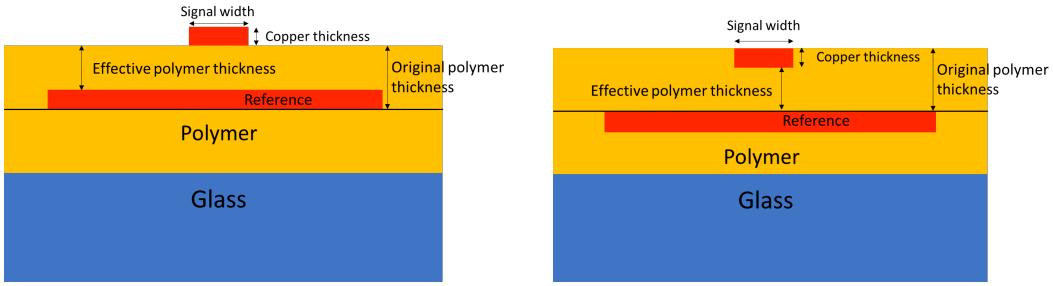


Figure 3.1: Schematic cross section of microstrip line on glass interposer, fabricated by SAP method (left) and embedded method (right)

Table 3.1: Impedance matched microstrip line design parameters

Effective dielectric thickness (μm)	Copper thickness (μm)	Signal width by SAP method (μm)	Signal width by embedded method (μm)
0.653	2	2	
0.887	2		2
3	2	7.5	6.64
8	2	19.35	18.2
13	2	31.4	30.08

3.1.2 Stripline Design

Stripline has two return paths and occupies 3 metal layers, as shown in Figure 3.2. Only symmetric stripline is considered in this research. The effective polymer thickness is equal to double the original polymer thickness minus the copper thickness. The EM field is shielded in the polymer dielectric by the return metal plane, experiencing homogeneous dielectric property. The approximate expression for Z_0 is much simpler than that of the microstrip line, as shown below:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} ln\left[\frac{4H}{0.67\pi W\left(0.8 + \frac{T}{W}\right)}\right] \tag{3.3}$$

In (3.3), ε_r is the polymer relative dielectric constant, H is the effective polymer thickness, W is the signal trace width, and T is the signal trace thickness. From the design aspect, the stripline geometry by the SAP method is identical to that processed by the embedded method. The stripline 2D extractor model with the same sweep frequency range and error tolerance was established to calculate the stripline geometry for impedance control at 5.8 GHz. The calculated impedance controlled symmetric stripline parameters are shown in Table 3.2.

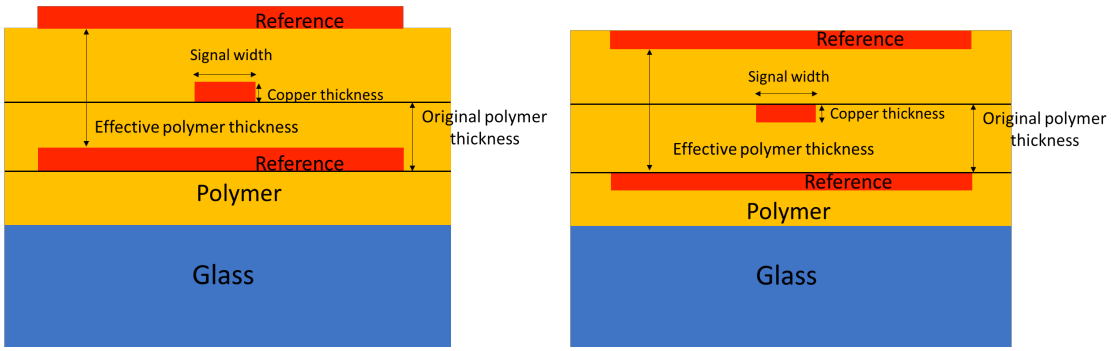


Figure 3.2: Schematic cross section of stripline on glass interposer, fabricated by SAP method (left) and embedded method (right)

Table 3.2: Impedance matched stripline design parameters

Effective dielectric thickness (µm)	Copper thickness (µm)	Signal width (µm)
6.26	3	2
8	2	2.94
18	2	8.73
28	2	14.7

3.1.3 CPW Design

The CPW transmission line only requires one metal layer, as shown in Figure 3.3. A stack of two dielectric materials (glass and polymer) are present in the CPW design, and the effective polymer thickness for the SAP method is equal to the original polymer thickness, while the embedded trace has less effective polymer thickness (original thickness minus the copper thickness). Therefore, no approximate expressions exist to calculate the impedance. The glass was assumed to be borosilicate glass (EN-A1 from Asahi Glass Company Japan), with a relative dielectric constant of 5.3, and loss tangent of 0.004. The 2D extractor model is the only way to accurately extract the impedance of CPWs on the glass interposer. Two different copper thicknesses for the two fabrication

methods were considered. The impedance controlled CPW parameters calculated by the 2D extractor model are shown in Table 3.3. For a similar geometry, the capacitive coupling for the SAP fabricated CPW is weaker than that of the embedded CPW due to the lower amount of polymer around the copper traces. As a result, thick copper design (5 µm) is preferred for SAP CPW to reduce the fabrication challenges. However, for the embedded trace method, the signal-to-ground gap is not a significant challenge, and 2 µm copper thickness was chosen for impedance matched design. The glass substrate has a higher dielectric constant than the ABF polymer. For CPW with wider signal to ground gap and thinner polymer layer, the EM field penetrates through the polymer into the glass, providing stronger capacitive coupling between signal and ground. Hence, the CPW gap for thin ABF is wider than for thicker ABF.

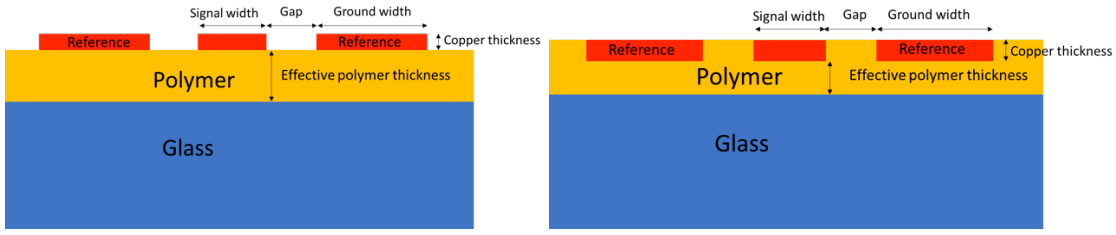


Figure 3.3: Schematic cross section of CPW on polymer laminated glass substrate, fabricated by SAP method (left) and embedded method (right)

Table 3.3: Impedance matched CPW design parameters

SAP method, copper thickness : 5 µm								
Effective polymer thickness: 5 µm			Effective polymer thickness: 10 µm			Effective polymer thickness: 15 µm		
Signal width (µm)	Gap (µm)	Ground width (µm)	Signal width (µm)	Gap (µm)	Ground width (µm)	Signal width (µm)	Gap (µm)	Ground width (µm)
3	2.1	20	3	2.09	20	3	2.09	20
5	2.47	20	5	2.44	20	5	2.43	20
10	3.33	40	10	3.22	40	10	3.19	40
15	4.13	60	15	3.91	60	15	3.84	60
Embedded method, copper thickness : 2 µm								
Effective polymer thickness: 3 µm			Effective polymer thickness: 8 µm			Effective polymer thickness: 13 µm		
Signal width (µm)	Gap (µm)	Ground width (µm)	Signal width (µm)	Gap (µm)	Ground width (µm)	Signal width (µm)	Gap (µm)	Ground width (µm)
3	1.475	20	3	1.456	20	3	1.454	20
5	1.81	20	5	1.762	20	5	1.756	20
10	2.607	40	10	2.448	40	10	2.417	40
15	3.363	60	15	3.075	60	15	3.003	60

3.2 The Root Cause of Process Variations

The SAP method was originally developed for board level fabrication as a superior alternative to the incumbent subtractive etch process. The emerging embedded trace method was inspired from wafer level BEOL process, with the trenches and vias formed by laser drilling or by lithography process in photo sensitive polymers. The process flows of all three methods are shown in Figure 3.4. The photolithography process for transferring the pattern from the designed photo mask to the photoresist on the substrate is present in subtractive and semi-additive processes, and also in the embedded method when using photo sensitive dielectric polymers. The copper etch process for the subtractive method is isotropic, resulting in severe undercut for high aspect ratio structures. Using a spray etch tool instead of immersion etching can improve the etch selectivity in the vertical direction over the lateral direction, and reduce the side wall etch

amount, but undercut cannot be eliminated. The SAP method starts with a very thin blanket copper layer called the seed layer. This seed layer can be deposited by either physical vapor deposition (PVD) or electroless plating, with typical thicknesses in the few hundred nanometer range. The photoresist is then deposited by spin or spray coating, or by dry film lamination on the copper seed layer. The designed copper pattern is formed by electrolytic plating in the open areas of the imaged and developed photoresist. The photoresist must be thicker than the target copper thickness to avoid over-plating. The photoresist is then stripped and the copper seed layer is etched. Since the copper seed layer is very thin compared to the total plated copper thickness, the etch time is much shorter than the subtractive process, which significantly reduces the copper side wall etch amount compared to the subtractive method. For the embedded method, the trenches and via holes for RDL can be drilled by UV laser or excimer laser if the dielectric polymer is non-photosensitive, such as ABF. Photo sensitive polymers are being developed by many groups as an alternative dielectric for the embedded method. For photosensitive materials, the via holes have to be formed by lithography first, followed by another polymer lamination and trench formation by another lithography step. No copper seed layer etch process is required for the embedded method, which is a significant advantage over the SAP method for ultra-fine RDL fabrication.

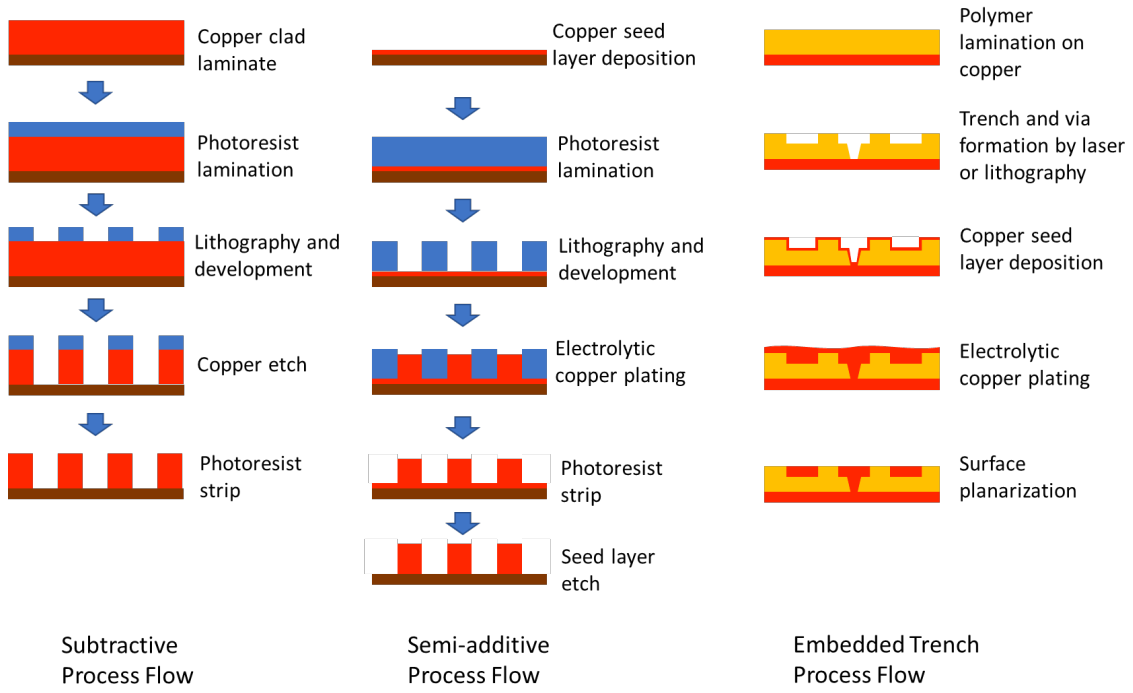
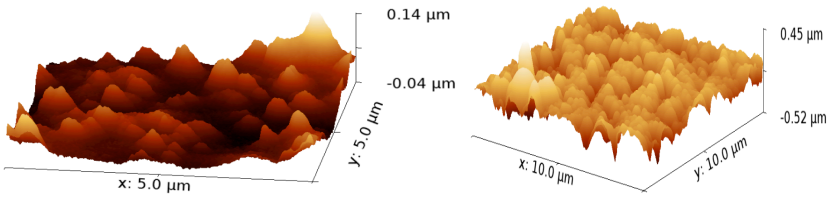


Figure 3.4: Subtractive method (left), semi-additive method (middle) for single layer RDL fabrication, and embedded method (right) for traces and via fabrication

The SAP method has advanced to 2 µm critical dimensions (CD) for interposer fabrication [33], and offers potentially lower cost than the wafer level BEOL process, which is commonly employed for silicon interposer fabrication. The laser embedded trench method was demonstrated [34] with 2 µm technology on selected dielectric materials, showing better line width control than the SAP method. The emerging photo sensitive polymer based embedded trench has demonstrated initial feasibility of scaling to 1.5 µm [27], but has other challenges such as poor adhesion strength and relatively high electrical loss at high frequencies. However, all these processes induce a finite amount of process variations, resulting in non-ideal line shapes for the copper traces. The detailed analysis of the source of process variations is discussed in the following sub-sections.

3.2.1 Copper Seed Layer Electroless Plating

The copper seed layer can be directly deposited on the polymer surface by electroless copper plating method, which is a low temperature, wet process with panel processability. Typically, the original polymer surface is very smooth, not ideal for strong copper adhesion. To enhance the adhesion for the required reliability, a wet etch process with permanganate solution is applied to roughen the polymer, called the "desmear" process. The AFM images of ABF dielectric polymer surface before and after the desmear process is shown in Figure 3.5. The average surface roughness value (R_a) increased from 15 nm to 75 nm. The copper seed layer bottom boundary follows the topography of polymer surface with the same surface roughness. This interface roughness affects the electrical performance, which is discussed later in this chapter.



R_a=15 nm **R_a=75 nm**

R_z=180 nm **R_z=1 µm**

Figure 3.5: AFM image of dielectric polymer surface before (left) and after (right) desmear process

3.2.2 Photolithography

The photolithography process is a dominant process used for transferring the designed pattern from the mask to the substrate. The dry film resist (DFR) commonly applied to board level fabrication is a negative tone material. In general, the resolution of

negative tone DFR is lower than the liquid positive photoresist applied in wafer level processing, but is more cost-effective for panel-level processing.

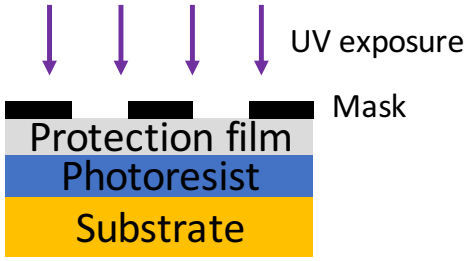


Figure 3.6: Contact mode lithography on DFR resulting in proximity mode

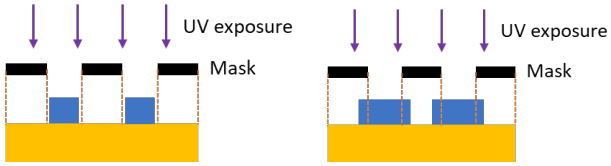


Figure 3.7: Under exposure (left) and over exposure (right) of the grating pattern

Due to the light diffraction and the low transparency of the dry film resist, the photolithography process cannot perfectly transfer the pattern from the mask to the photoresist. The DFR has a transparent protection film on the resist layer during exposure, showing in Figure 3.6. With contact mode for the mask aligner, the gap between the mask and the resist layer causes the diffraction of light at the edge of an opaque feature on the mask as the collimated UV beam passes through the clear area. Therefore, the lithography type is proximity for DFR, and the light intensity in the opaque area is not zero. If the exposure time is increased until the cumulated energy in the opaque area is above the threshold energy of a negative tone photoresist, then more of the resist remains after the development. On the contrary, if the accumulated energy in the clear area is below the threshold energy due to short exposure time, less of the resist remains, as

shown in Figure 3.7. This variation leads to wider or thinner copper traces after metallization. Furthermore, the thickness of typical DFR is larger than liquid positive photoresists. With the limited transparency, the exposure intensity across the resist layer in the vertical direction is non-uniform. The cumulative dose near the photoresist-to-substrate interface is lower than at the top surface of the photoresist. After development, the cross-sectional view of the photoresist traces looks like upside down trapezoids, as shown in Figure 3.8. This results in trapezoidal shaped copper traces after electrolytic plating. However, depending on the development method, when the feature size is smaller than a certain value, the exposed photoresist may not be fully dissolved in the developing solvent, resulting in an opposite shape with a wider bottom instead (Figure 3.8). The lithography on the photo sensitive polymer for the embedded trench method has similar process variations, which also leads to trapezoidal shaped traces and tapered vias.

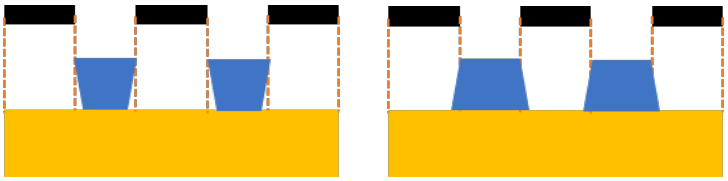


Figure 3.8: Upside down trapezoidal shape of photoresist after fully development due to the non-uniform exposure dose across the vertical direction (left) and trapezoidal shape of photoresist if not fully developed due to tight feature size (right)

3.2.3 Electrolytic Copper Plating

The copper RDL structures on the build-up layer are metallized by electrolytic copper plating. The copper thickness is determined by the plating time and current density, which can be calculated theoretically using the following equation,

$$T = \frac{M_w I t}{2FA\rho} \tag{3.4}$$

where T is the copper deposit thickness in cm, M_w is the copper molar mass (63.546 g/mol), I is the plating current (ampere), t is the plating time (second), F is the Faraday constant (96485.3329 c/mol), A is the area of the deposit in cm^2, and ρ is the copper density (8.96 g/cm^3). Due to the variation in local plating current densities, the thickness of plated copper structures may not be uniform across the panel, leading to copper thickness variations for the SAP method. This thickness non-uniformity can be resolved by surface planarization, which is discussed in Chapter 4.

3.2.4 Copper Seed Layer Etching

The copper seed layer etching process is the last step for RDL metal layer fabrication. This critical step has a great impact on the copper line shape integrity. The conventional method is the isotropic immersion wet etching. The copper side wall etch amount is close to the thickness of copper seed layer. However, the seed layer etching time extends at narrow spaces such as gap between copper traces, since the etchant can be "trapped" in such confined area. This extended etching time leads to undercut and over etch on copper traces, leaving narrower and trapezoidal shaped traces with rough copper surface roughness, or even trace lift-off. The rough copper traces after seed layer etch is shown in Figure 3.9. To improve the copper trace quality after seed layer etching, an adequate selectivity of seed layer over plated copper is mandatory.

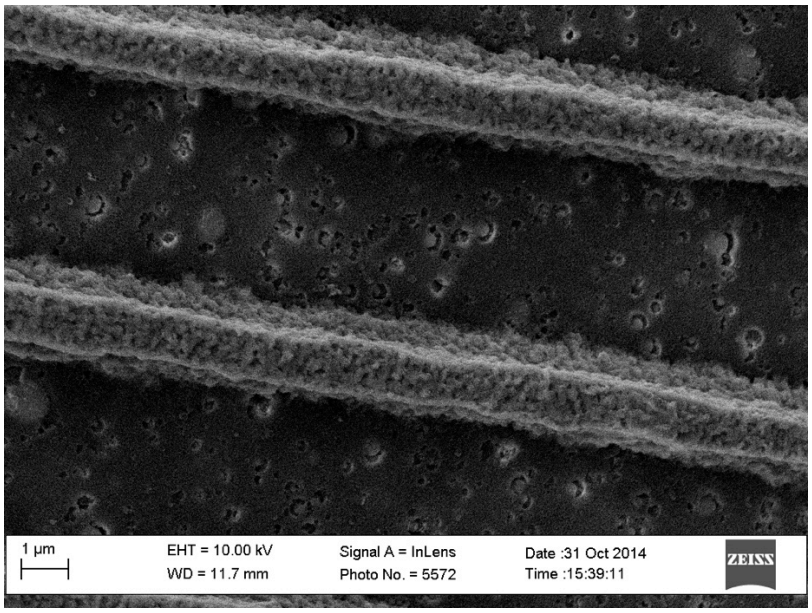


Figure 3.9: Roughened copper traces after seed layer etch

3.2.5 Polymer trench laser drilling

The laser trench formation process is the most critical process for the laser embedded trench method. It has been reported that the silica filler size in the polymer dielectric affects the trench profile and surface roughness [34]. Polymer materials with smaller filler size showed less trench side wall taper angle with lower surface roughness, while the polyimide without silica filler showed the best trench profile with smooth surfaces. The tapered side wall angle can be controlled by the laser power, and the trench depth can be controlled by the number of laser pulses for a certain laser power. After metallization, the trench surface roughness will be transferred to copper trace bottom and side wall roughness. Finally, the copper overburden on the surface is removed by planarization, and this planarization process may remove excessive polymer with copper, resulting in thinner polymer and copper traces.

3.3 Electrical Performance Impact due to Process Variations

The previous sub-section analyzed the root cause of major process variations. To analyze the RDL trace electrical performance, four critical process variations for SAP method and embedded method were chosen. These are: (1) copper trace width, (2) copper thickness, (3) side wall taper, and (4) copper surface roughness, as illustrated in Figure 3.10. Microstrip line, stripline, and CPW were analyzed in detail individually.

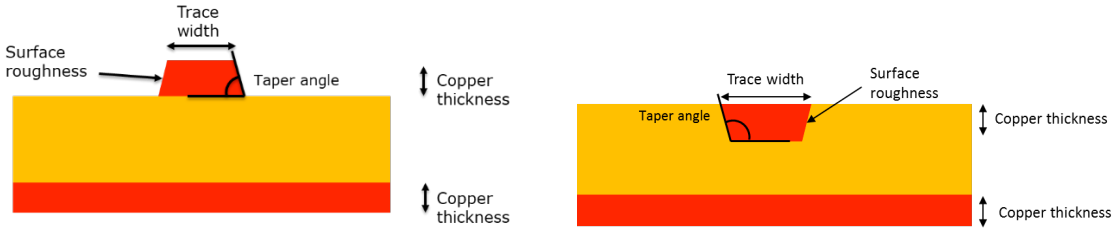


Figure 3.10: Four typical process variations for copper RDL by SAP method (left) and embedded method (right)

3.3.1 Transmission Lines Selected for RLGC Analysis

3.3.1.1 Microstrip Line

Microstrip line is a common type of transmission line used in a package, with a signal trace on top of the dielectric layer, and a much wider plane for the return path under the dielectric layer. The common distributed circuit model with parasitic resistance (R), inductance (L), capacitance (C), and conductance (G) for microstrip line can be extracted from a 2D extractor model, the same one used for verifying the impedance controlled design in the previous sub-section. The side view of a microstrip line with RGLC parasitic parameters is shown in Figure 3.11. The parasitic inductance is determined by the magnetic flux around a conductor per ampere of current through it. For

a fixed current, the magnetic flux outside the conductor is fixed, but varies inside the conductor. If the current flows only on the edge of the conductor at higher frequencies, the magnetic flux inside the conductor is close to zero, leading to lower inductance compared to lower frequencies where the magnetic flux is not zero due to the evenly distributed current inside the conductor. At low frequencies, the inductance and resistance is dominated by the narrow signal path. When frequency increases, the current tends to flow along the lowest inductance path, limiting the cross-sectional area where the current is distributed. Therefore, the resistance increases, but the inductance decreases. The simulated current distribution in microstrip lines fabricated by SAP method at 1 GHz and 30 GHz are shown in Figure 3.12. The signal trace is 7.5 μm wide, 2 μm thick, and the ABF GX92P dielectric has the effective thickness of 3 μm. According to the result, at the lower frequency (1 GHz), the signal current is evenly distributed in the signal trace, and the return current is located under the signal current, occupying a large cross-sectional area. When the frequency increases to 30 GHz, the signal current mainly flows at the edge of the signal trace, and the return current is located in a thin layer on top of the return plane, under the signal path. The capacitive coupling between the signal and return path contributes to the parasitic capacitance, which is directly proportional to the dielectric constant of the material between two conductors. The leakage current between two conductors under applied voltage is the parasitic conductance, which is proportional to the loss tangent of the dielectric material.

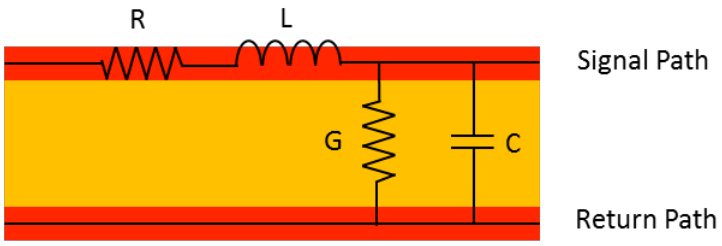
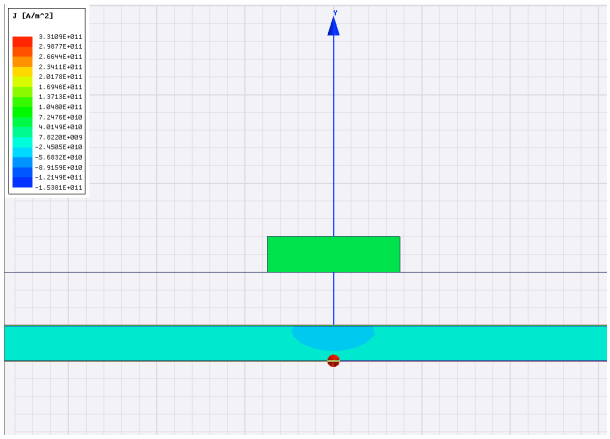
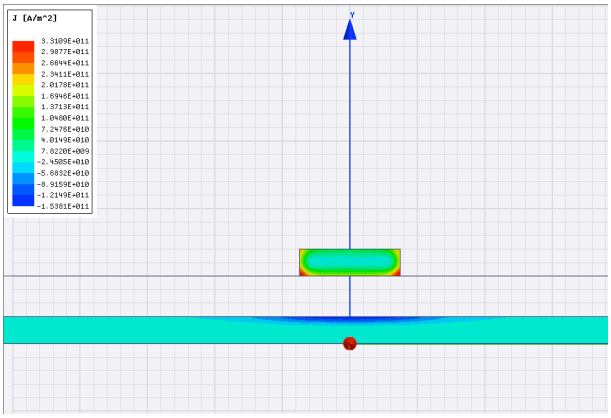


Figure 3.11: Microstrip line side view with distributed RLGC



(a)



(b)

Figure 3.12: Simulated current distribution of microstrip line with 7.5 µm line width, 2 µm thickness, and 3 µm ABF GX92P as dielectric layer, at (a) 1 GHz and (b) 30 GHz

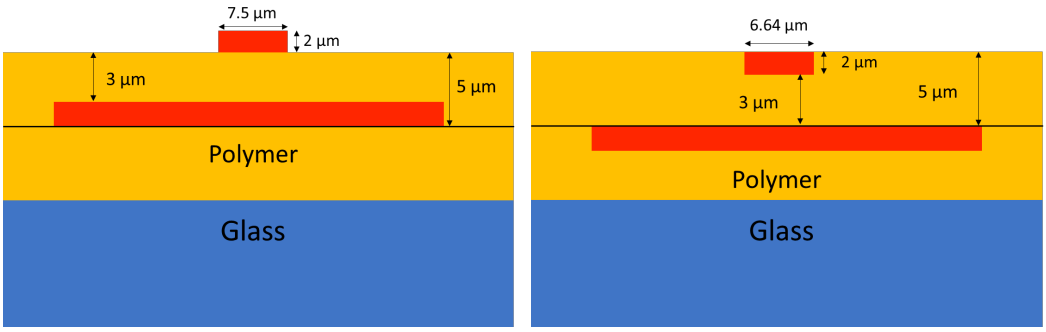


Figure 3.13: Dimensions of the microstrip lines fabricated by SAP method (left) and embedded method (right) for process variation analysis

The finest microstrip line design from section 3.1.1 was chosen to study the four major process effects on parasitic RLGC, with the dimensions shown in Figure 3.13. Detailed analysis of RLGC is discussed in section 3.2.2.

3.3.1.2 Stripline

Stripline is another common transmission line used in package design. The center signal conductor is sandwiched between dielectric layers on both sides and a pair of ground planes, one on top and the other on the bottom. The side view of a stripline with RGLC parasitic parameters is shown in Figure 3.14. The signal path is capacitively coupled with both top and bottom return paths (ground planes). The effective dielectric constant is equal to the material dielectric constant. The parasitic capacitance is the sum of C_1 and C_2, and the parasitic conductance is the sum of G_1 and G_2. The parasitic resistance and inductance is mainly dictated by the much narrower signal path, similar to the microstrip line. The finest stripline design in the previous section was chosen to study the four major process effects on parasitic RLGC. The detailed dimension is shown in

Figure 3.15, with no dimensional difference between SAP method and embedded method due to symmetry.

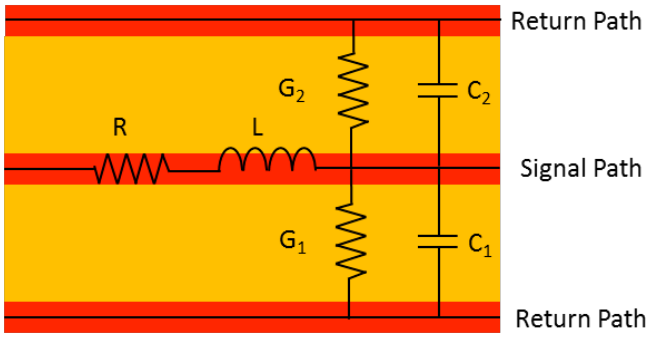


Figure 3.14: Stripline side view with distributed RLGC

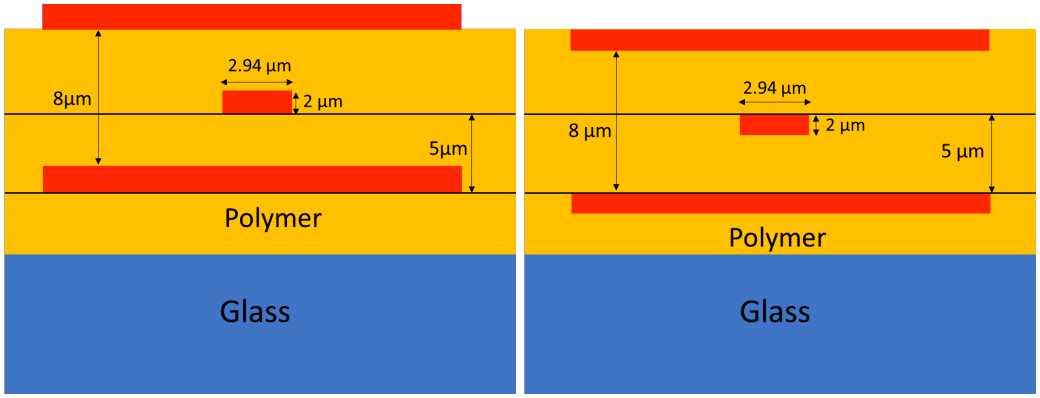


Figure 3.15: The dimensions of the stripline fabricated by SAP method (left) and embedded method (right) for process variation analyze

3.3.1.3 CPW

The signal path of CPW transmission line is sandwiched by two much wider copper traces that serve as the return path. The cross-sectional views of CPW fabricated by SAP and embedded methods are shown in Figure 3.16. The effective dielectric constant is a complex mix of air, polymer, and the substrate dielectric constant, which can only be accurately calculated by a 2D extractor. For SAP fabricated CPW, the

leakage current only flows through the bottom boundary of copper traces, while for the partially embedded CPW, the leakage current flows through the copper side wall in addition to the bottom boundary. Therefore, higher conductance can be expected for the embedded case. Similar to stripline which has two return paths, the parasitic capacitance for CPW is the sum of C_1 and C_2, and the parasitic conductance is the sum of G_1 and G_2. The parasitic resistance and inductance is also mainly dictated by the much narrower signal path. The dimensions of the impedance controlled CPW chosen for parasitic RLGC analysis are shown in Figure 3.17.

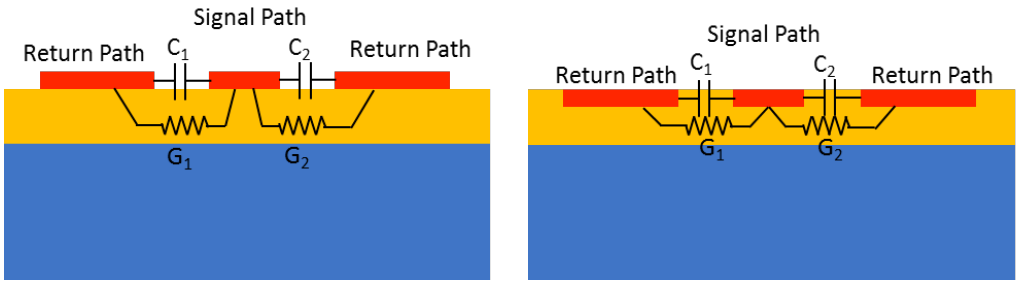


Figure 3.16: Cross section of CPW fabricated by SAP method (left) and embedded method (right) with distributed capacitance and conductance

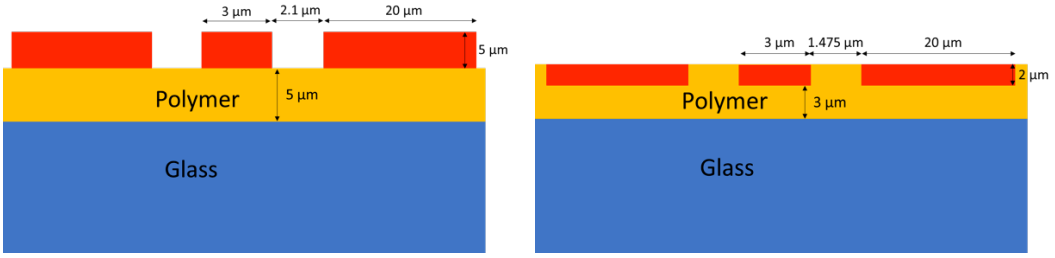


Figure 3.17: The dimensions of the CPW fabricated by SAP method (left) and embedded method (right) for process variation analyze

3.3.2 Copper Trace Width Variation

The copper trace width variation is mainly caused by lithography and copper seed layer etch steps for the SAP method and by the laser trench formation step for the embedded method. For microstrip line fabrication by both methods, the overlapped area between signal path and return path decreases as the line width decreases, resulting in reduced capacitance. Furthermore, the leakage current also reduces, resulting in reduced conductance. Reducing the cross-sectional area of the conductor increases the external magnetic flux, which increases the inductance. Therefore, when the copper trace width is reduced, the parasitic inductance increases. Due to the reduced conductor cross-sectional area, the resistance increases as well. For a microstrip line fabricated by the SAP method with widths of 5.5 μm, 6.5 μm, 7.5 μm, and 8.5 μm, the RLGC were simulated up to 30 GHz, shown in **Figure 3.18**, where the 7.5 μm width is the 50-ohm impedance matched design point at 5.8 GHz. The same analysis was also carried out for embedded trench microstrip lines with widths of 4.64 μm, 5.64 μm, 6.64 μm, 7.64 μm, and 8.64 μm, where the 6.64 μm width had a 50-ohm characteristic impedance at 5.8 GHz. The simulated partially embedded microstrip line RLGC is shown in Figure 3.19.

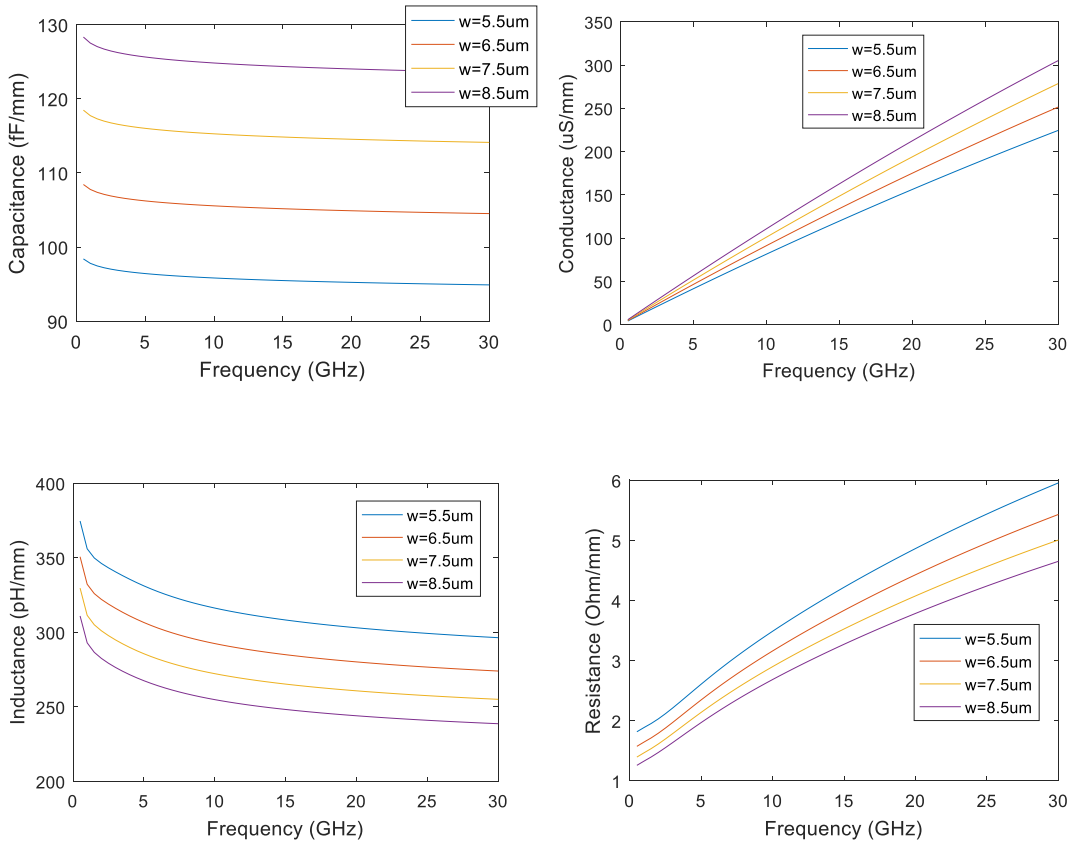


Figure 3.18: Simulated capacitance, conductance, inductance, and resistance per unit length of microstrip line with different width fabricated by SAP method

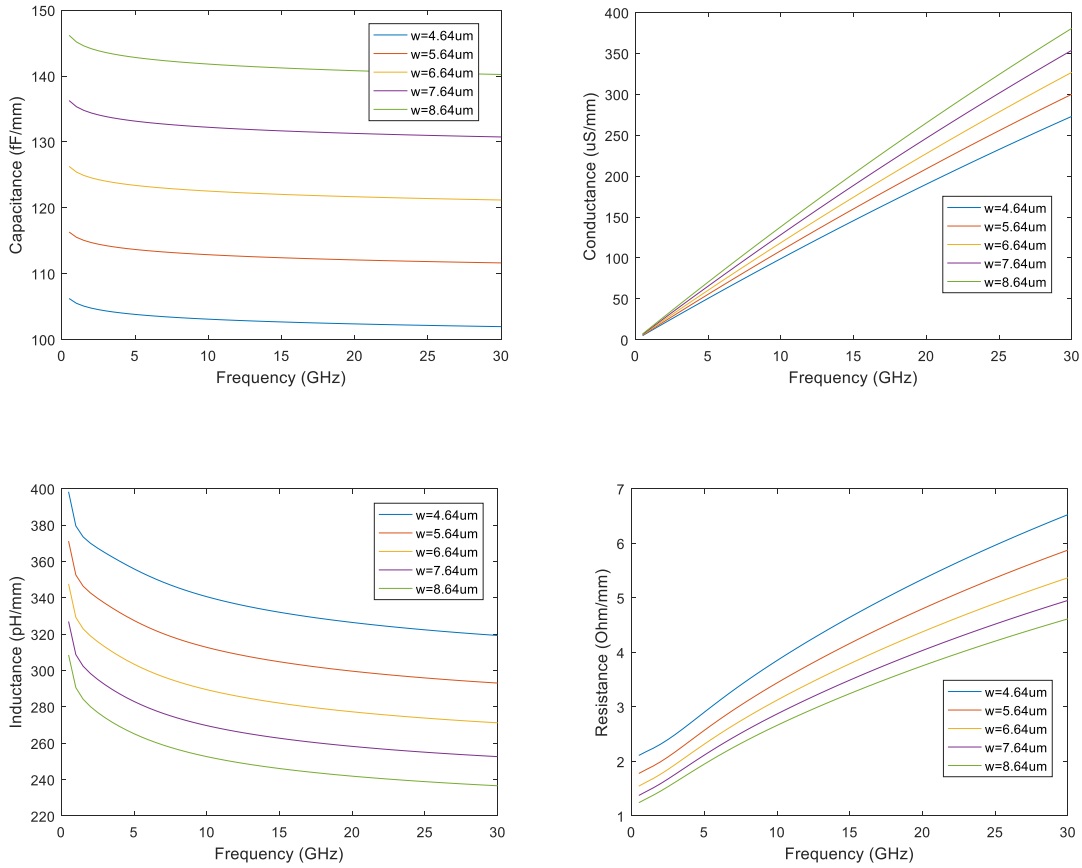


Figure 3.19: Simulated capacitance, conductance, inductance, and resistance per unit length of microstrip line with different width fabricated by embedded method

For striplines, SAP and embedded methods share the same 2D extractor model. Similar to the microstrip line, narrower signal trace width results in smaller capacitance, smaller conductance, higher inductance and higher resistance. For striplines with widths of 0.94 µm, 1.94 µm, 2.94 µm, and 3.94 µm, the RLGC were simulated up to 30 GHz, shown in Figure 3.20, where 2.94 µm width is the 50-ohm impedance matched design at 5.8 GHz. The simulation results showed the same trend as the qualitative analysis.

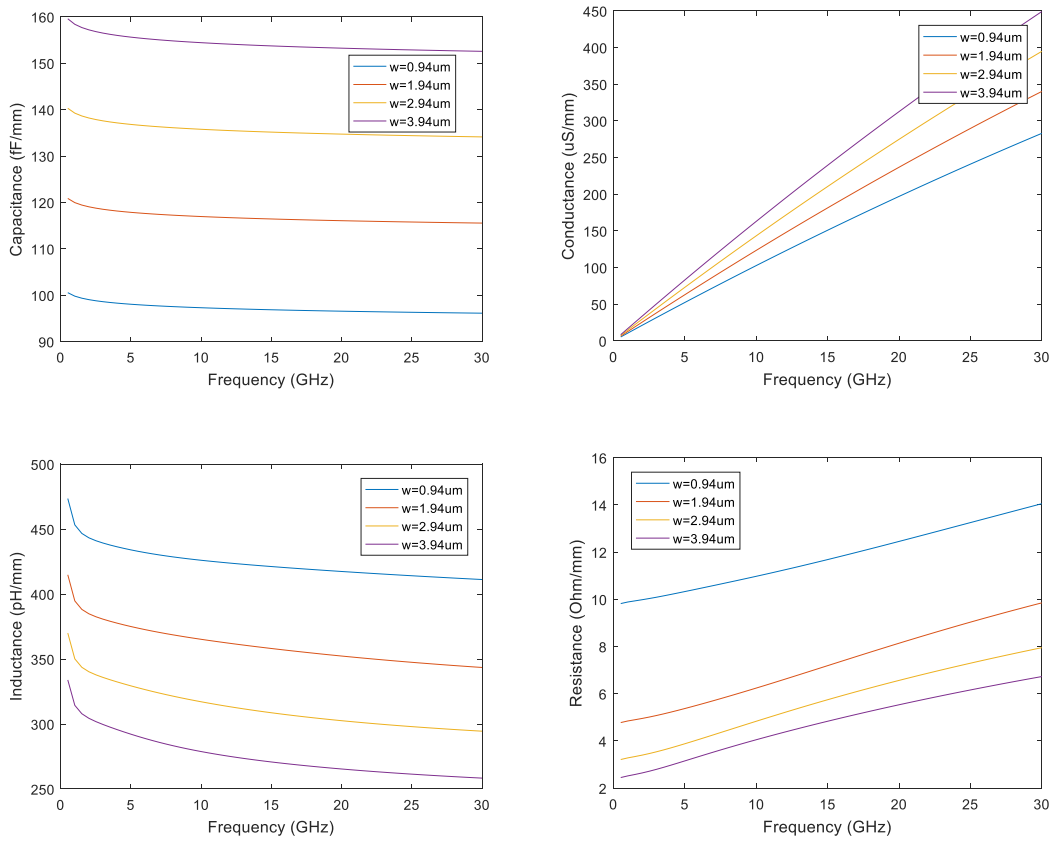


Figure 3.20: Simulated capacitance, conductance, inductance, and resistance per unit length of stripline with different width

In the CPW case, the gap between the signal and ground traces increases when the trace widths reduce, to maintain the same line pitch. The sum of signal width and gap was set to be a constant number. The larger gap between signal and ground traces results in weaker capacitive coupling, and in a longer path for the leakage current to flow, leading to lower capacitance and conductance. The parasitic inductance is the self-inductance of signal path plus the return path minus the mutual inductance. The inductance increases as the self-inductance of signal trace increases due to the smaller cross-sectional area. The mutual-inductance also decreases due to the larger gap between the signal and ground

traces. The resistance increases with reducing width for the electrical current passing through the smaller cross-sectional area. For CPWs fabricated by the SAP method with widths of 1 μm, 2 μm, 3 μm, and 4 μm, the simulated RLGC is shown in Figure 3.21, where 3 μm width is the 50-ohm impedance matched design at 5.8 GHz. The embedded CPW case is shown in Figure 3.22. It can be seen that the capacitance and conductance increases significantly when the gap is very small (<1 μm) for the embedded case. Furthermore, larger cross-sectional area does not guarantee lower resistance at high frequency. With a narrow gap, the area over which the electrical current is distributed may be even smaller than with a wider gap and narrower trace. For partially embedded CPW, the resistance of 4 μm wide with 0.475 μm gap is higher than 3 μm wide CPW with the gap of 1.475 μm beyond 7 GHz.

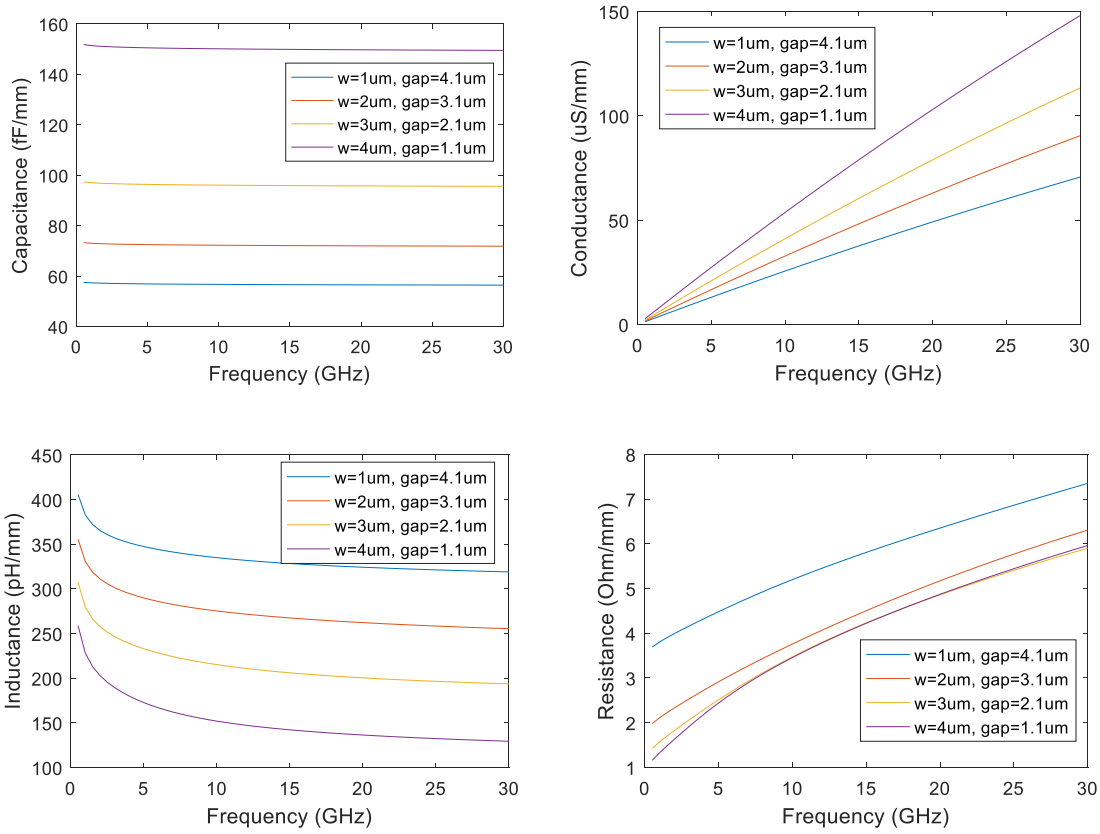


Figure 3.21: Simulated capacitance, conductance, inductance, and resistance per unit length of CPW with different width and gap fabricated by SAP method

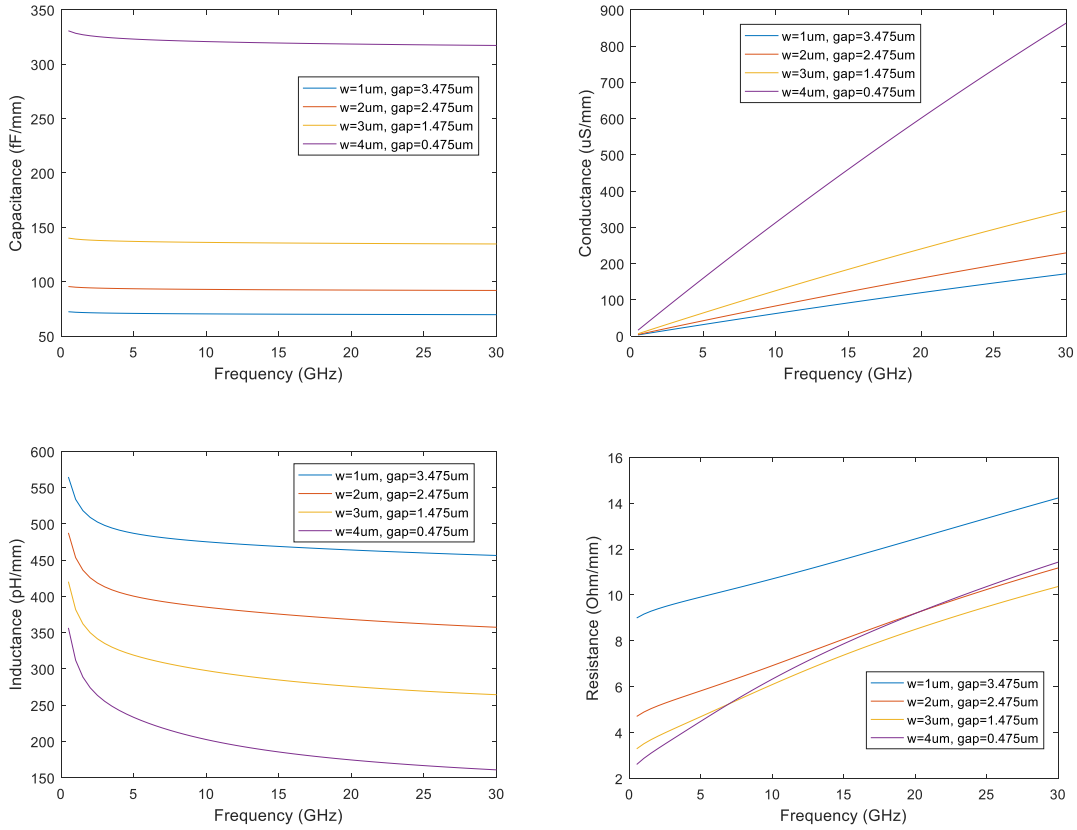


Figure 3.22: Simulated capacitance, conductance, inductance, and resistance per unit length of CPW with different width and gap fabricated by embedded method

To sum up, for all transmission line types, narrower signal trace width caused by seed layer over etch leads to lower capacitance, lower conductance, higher inductance, and higher resistance, and the opposite trends are true for wider signal traces caused by trench over drilling for the embedded method. However, for a given line pitch, the widening of the traces in the embedded method will cause the lines to be closer to each other, increasing parasitic signal cross-talk.

3.3.3 Copper Thickness Variation

The copper thickness is determined by the electrolytic copper plating current density and plating time for the SAP method, as discussed in Section 3.2.3. For the embedded method, the trench is fully metallized to form copper traces and planarized to remove overburden. The copper thickness is dependent only on the trench depth and the planarization process. To simplify the analysis, the effective dielectric thickness was assumed to be the original polymer thickness minus the copper thickness for microstrip lines and partially embedded CPW. The effective dielectric thickness for stripline was calculated as double the original polymer thickness minus the copper thickness. The SAP fabricated CPW transmission line has only one metal layer and there is no change in polymer thickness when the copper thickness varies. Therefore, except for the SAP fabricated CPW, thinner copper results in a thicker dielectric layer for all other transmission line cases.

For a microstrip line, the thicker dielectric layer reduces the capacitive coupling between signal and return paths, as well as the leakage current, resulting in lower capacitance and conductance. The parasitic inductance increases with reduced copper thickness for the microstrip line due to two main reasons. One is the reduced cross-sectional area of the conductor, which increases the overall magnetic flux per unit ampere around the line. The other is the reduced mutual inductance between signal and return paths with increased dielectric thickness separating the two conductors. The resistance also increases with reduced cross-sectional area. The RLGC of the microstrip line with 1 μm, 2 μm, and 3 μm copper thickness for both fabrication methods were simulated up to

30 GHz, shown in Figure 3.23 and Figure 3.24, where 2 µm copper thickness is the impedance matched design at 5.8 GHz.

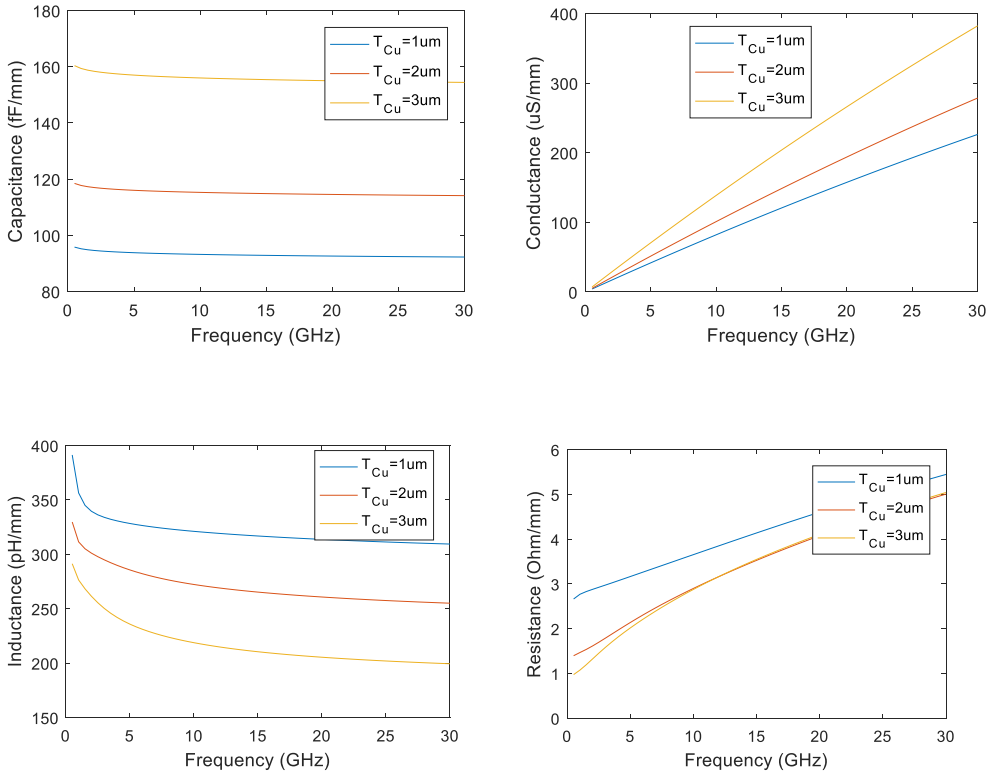


Figure 3.23: Simulated capacitance, conductance, inductance, and resistance per unit length of microstrip line with different copper thickness and dielectric thickness fabricated by SAP method

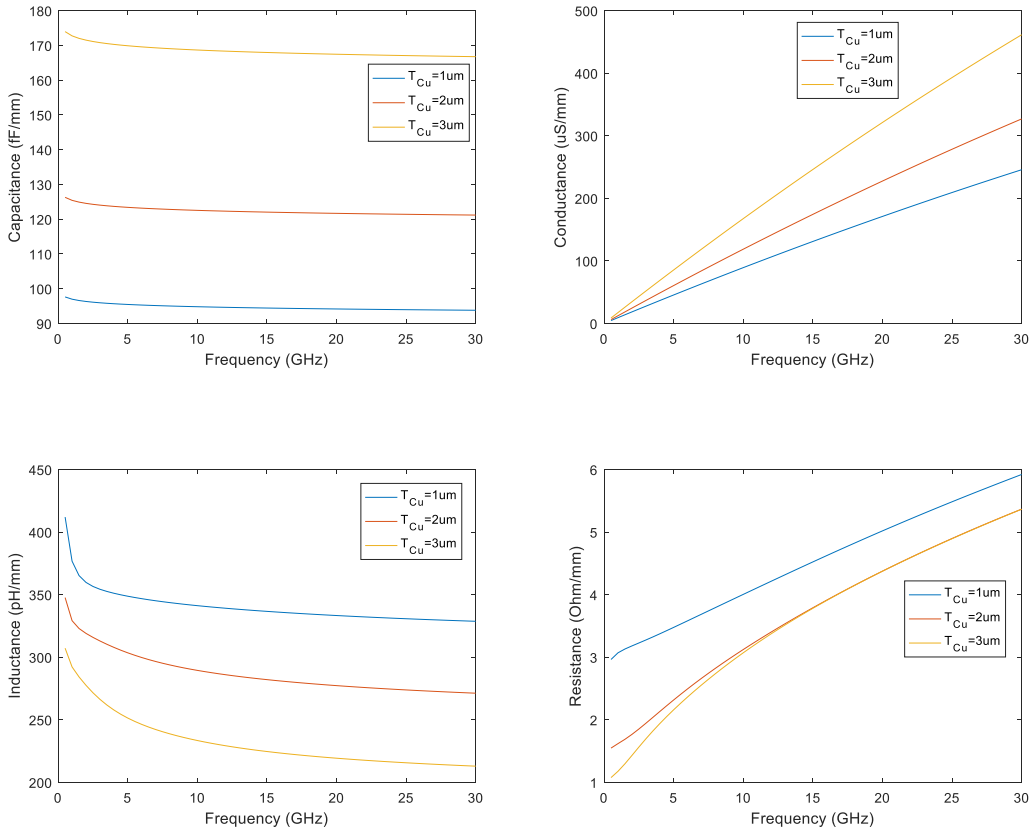


Figure 3.24: Simulated capacitance, conductance, inductance, and resistance per unit length of microstrip line with different copper thickness and dielectric thickness fabricated by embedded method

The RLGC for stripline follows a similar trend as the microstrip line, for the same reasons. Reducing copper thickness reduces the capacitance and conductance, but increases the inductance and resistance. The RLGC of the stripline with 1 µm, 2 µm, and 3 µm copper thickness were simulated up to 30 GHz, shown in Figure 3.25. The 2 µm copper thickness is the impedance matched design at 5.8 GHz.

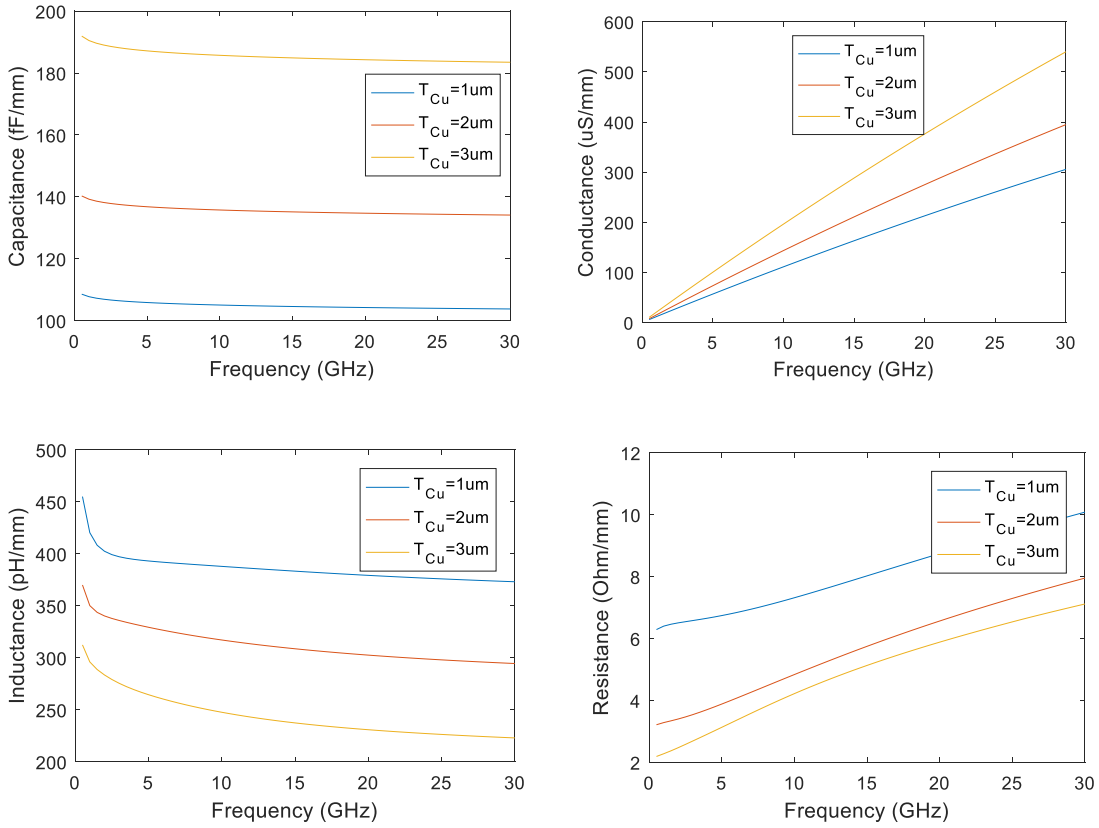


Figure 3.25: Simulated capacitance, conductance, inductance, and resistance per unit length of stripline with different copper thickness

For CPW, the copper thickness affects the overlap area between signal and ground traces. A thicker CPW has larger overlap area, leading to higher capacitance. For a partially embedded CPW, the conductance increases with copper thickness. However, the conductance is not affected for SAP fabricated CPW, due to same leakage current path. The inductance also increases with reduced copper thickness for both CPW cases mainly due to the increased self-inductance. The resistance increases when the thickness reduces, same as for the other transmission line types. The simulated RLGC of the SAP fabricated CPW with 4 µm, 5 µm, and 6 µm copper thickness is shown in Figure 3.26, with 5 µm copper thickness to be the impedance matched design at 5.8 GHz. For partially

embedded CPW, the copper thickness variation of 1 µm, 2 µm, and 3 µm were simulated, as shown in Figure 3.27, where the impedance matched design at 5.8 GHz has 2 µm copper thickness.

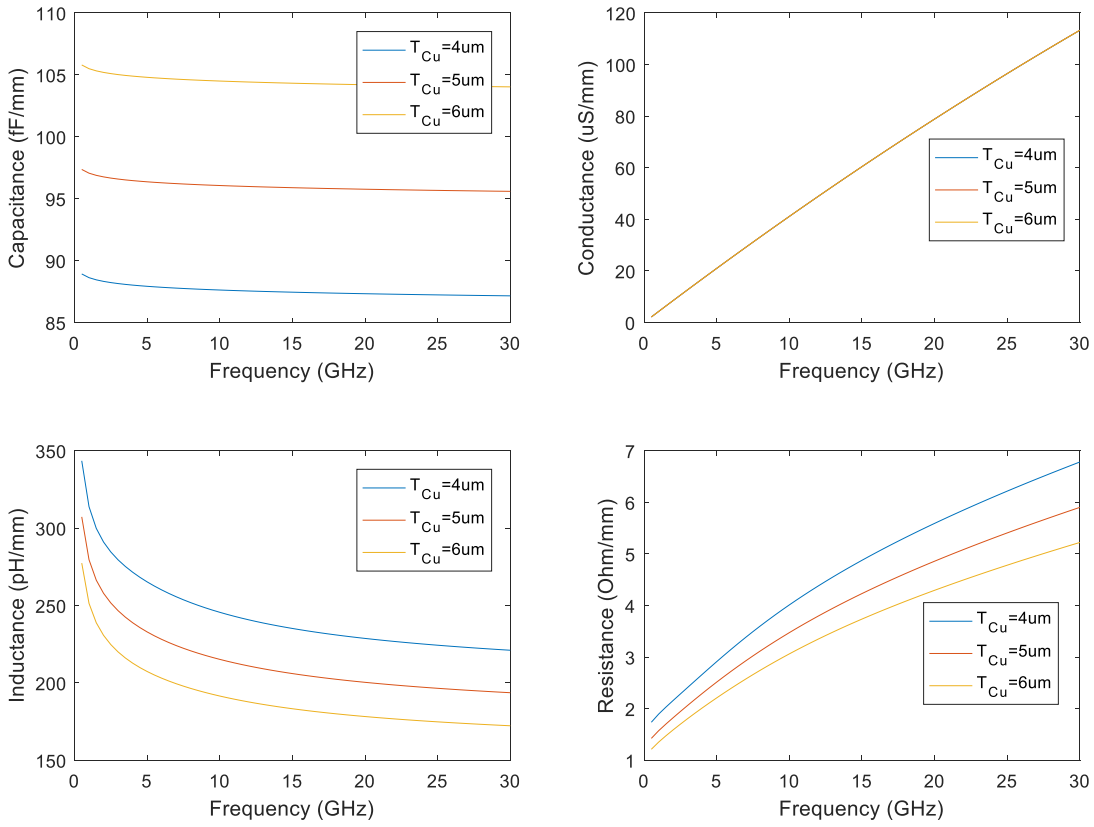


Figure 3.26: Simulated capacitance, conductance, inductance, and resistance per unit length of CPW fabricated by SAP method with different copper thickness

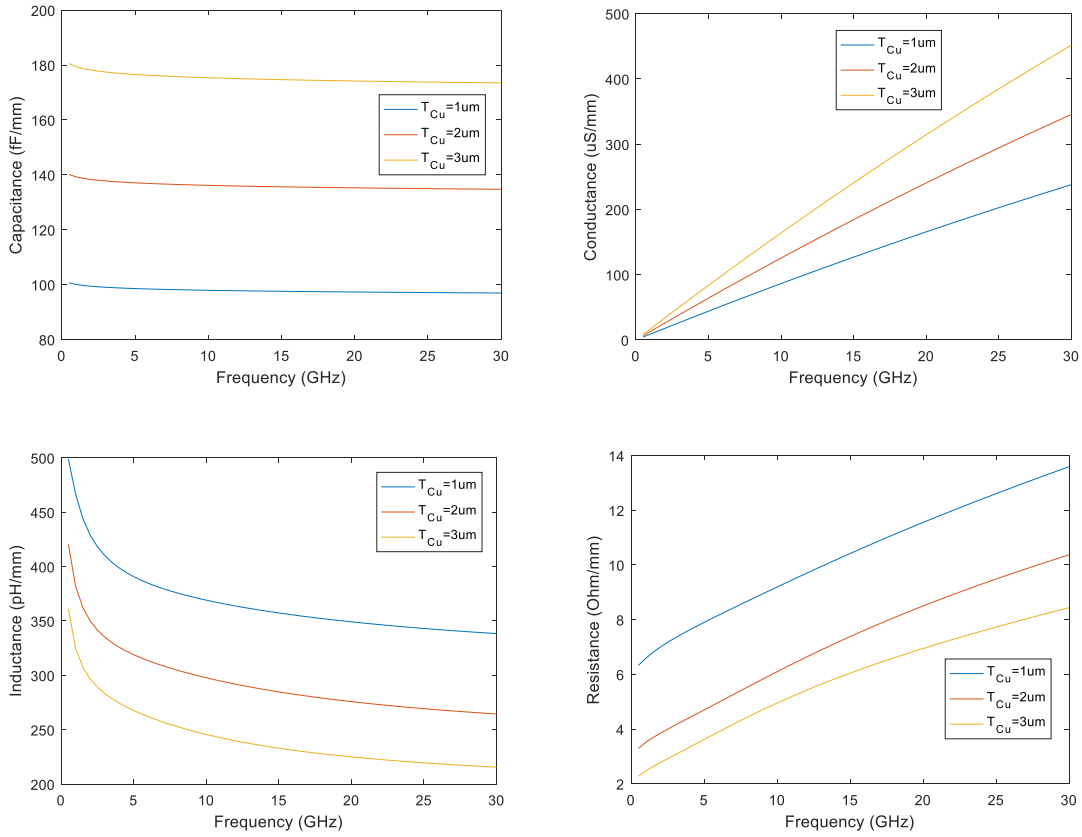


Figure 3.27: Simulated capacitance, conductance, inductance, and resistance per unit length of CPW fabricated by embedded method with different copper thickness

In summary, for all transmission line types, a thinner copper trace results in lower capacitance, lower conductance, higher inductance, and higher resistance.

3.3.4 Tapered Copper Side Wall

Non-uniform exposure intensity along the vertical direction during the lithography process for negative tone DFR or photo sensitive polymer leads to non-vertical side walls after development, as discussed in Section 3.2.2. For the SAP method, the metallized copper traces follow the shape and size of the gap between dry film resist

traces. The subsequent seed layer etch process makes the sidewall taper even worse. The laser drilled trench in polymer dielectric showed an upside down trapezoidal cross-sectional shape, with the taper angle determined by the polymer type and the laser power. The trench taper angle is transferred to copper trace taper angle after metallization. To simplify the analysis for the SAP method, the signal trace bottom width was fixed at the impedance matched design value, while the top width was tuned to create the tapered side wall. For the embedded method, W_top is fixed at optimum value instead, while W_bottom was set at different values to create upside down trapezoidal shaped line profiles.

For microstrip lines, the cross-sectional schematic of the simplified analysis is illustrated in Figure 3.28. In the SAP case, W_bottom was fixed at 7.5 μm, while W_top was tuned at 4.5 μm, 5.5 μm, 6.5 μm, and 7.5 μm. As for the embedded method, W_top was set at 6.64 μm, and W_bottom was varied at 3.64 μm, 4.64 μm, 5.64 μm, and 6.64 μm. The corresponding side wall angle for 2 μm thick copper is calculated in Table 3.4, which is defined as the angle between the base and side wall in the cross-sectional view. The RLGC of both microstrip line models were simulated up to 30 GHz, shown in Figure 3.29 and Figure 3.30. The tapered side wall reduces the effective copper trace width, which reduces the capacitive coupling, but not as significantly as copper trace width reduction. The capacitance is more sensitive for the partially embedded microstrip line than for the traditional one by the SAP method. The conductance remains unaffected due to the same physical contact area to the dielectric polymer for traditional microstrip line, while it reduces for partially embedded microstrip line due to reduced physical contact area. The inductance and resistance increases slightly when the cross-sectional area

decreases with tapered side wall. According to the simulation results, the parasitic RLGC are less sensitive to the copper trace tapered side wall angle than to the width variation.

Figure 3.28: Simplified tapered microstrip line analysis for SAP method (left) and embedded method (right)

Table 3.4: W_top and W_bottom variation and corresponding side wall taper angle for microstrip line

SAP method		Embedded method	
W_top variation (µm)	Side wall taper angle	W_bottom variation (µm)	Side wall taper angle
7.5	90°	6.64	90°
6.5	76°	5.64	104°
5.5	63.4°	4.64	116.6°
4.5	53.1°	3.64	126.9°

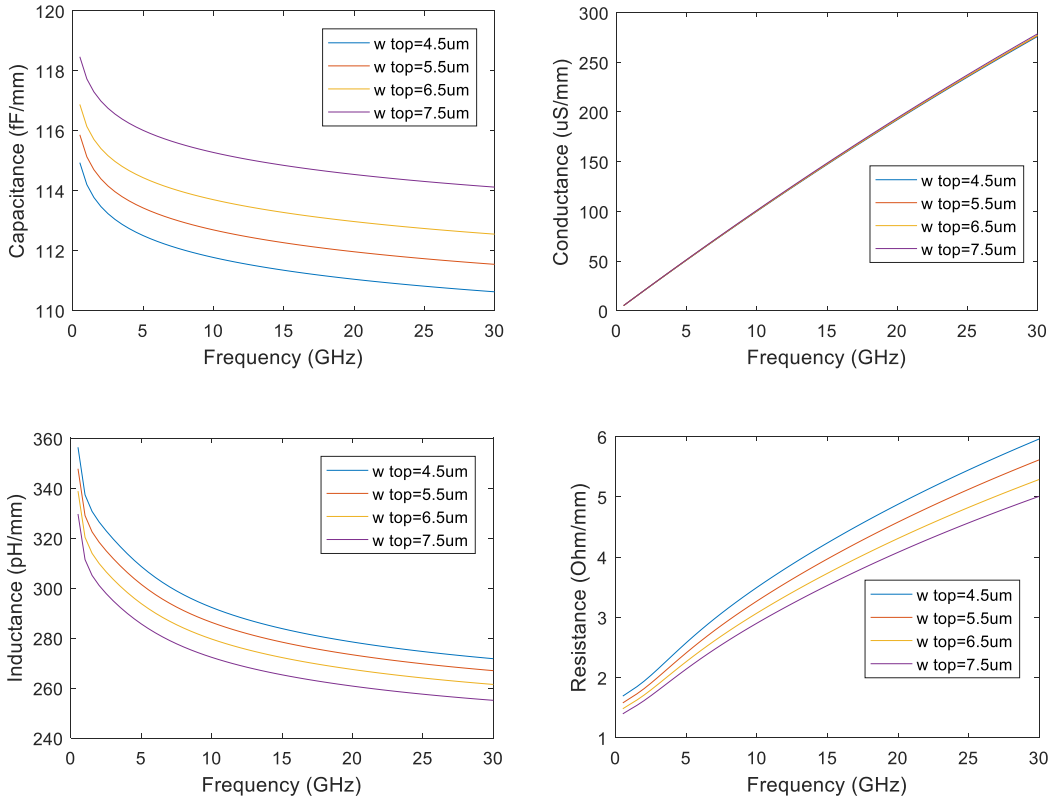


Figure 3.29: Simulated capacitance, conductance, inductance, and resistance per unit length of microstrip line with different copper trace top width on fixed bottom width, fabricated by SAP method

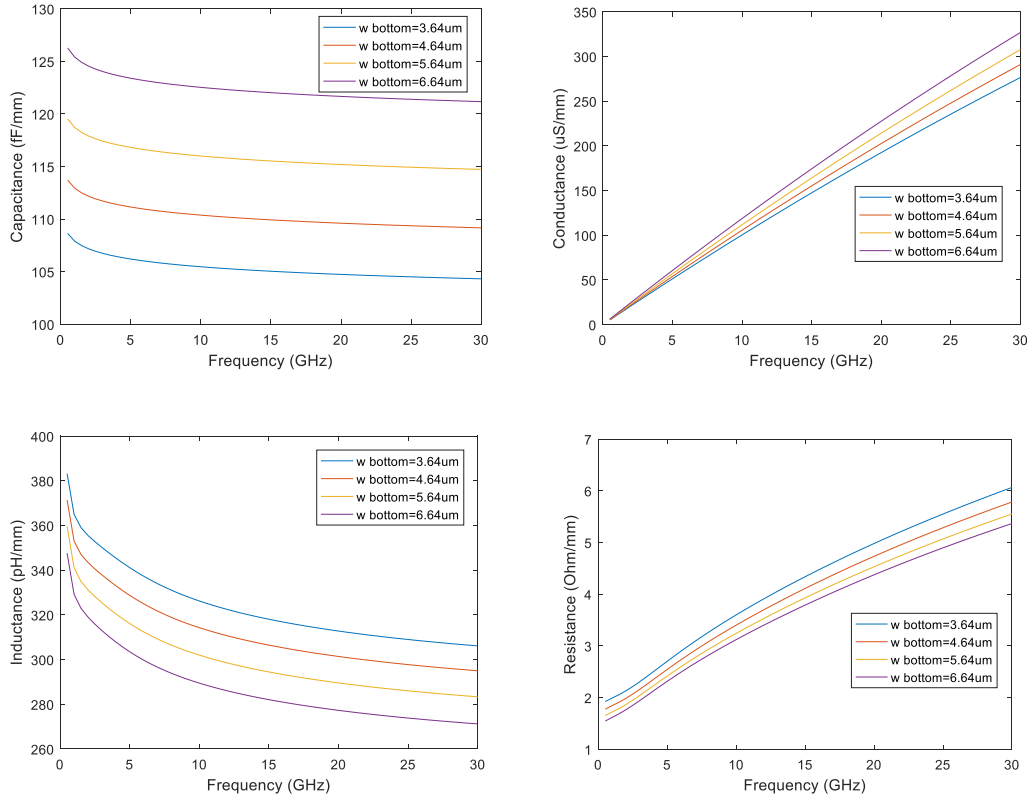


Figure 3.30: Simulated capacitance, conductance, inductance, and resistance per unit length of microstrip line with different copper trace bottom width on fixed top width, fabricated by embedded method

For stripline, the cross-sectional schematic for the simplified analysis is illustrated in Figure 3.31. The SAP fabricated stripline has W_bottom larger than W_top, while for stripline fabricated by the embedded method, W_bottom is smaller than W_top. Due to symmetry, the 2D modeling for the two different fabrication methods for width and thickness variation analysis can be shared. Therefore, the SAP stripline model was chosen for this analysis. W_bottom was fixed at 2.94 µm, while W_top was tuned at 0.94 µm, 1.94 µm, and 2.94 µm. The corresponding side wall angle for 2 µm thick copper is shown in Table 3.5. The taper angles are the same as for the microstrip line analysis,

except for the smallest angle model. The simulated RLGC is shown in Figure 3.32. Similar to the microstrip line, the tapered wall reduces the effective copper width, resulting in lower capacitance. The conductance slightly decreases with taper angle for a fixed bottom width. With the smaller cross-sectional area of the tapered model, the inductance is higher, and so being the resistance.

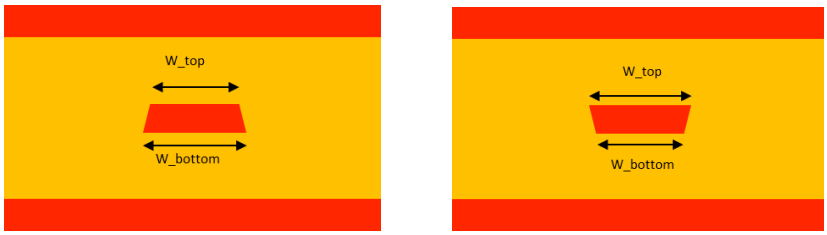


Figure 3.31: Simplified tapered stripline analysis for SAP method (left) and embedded method (right). Due to symmetry, only SAP method model is analyzed.

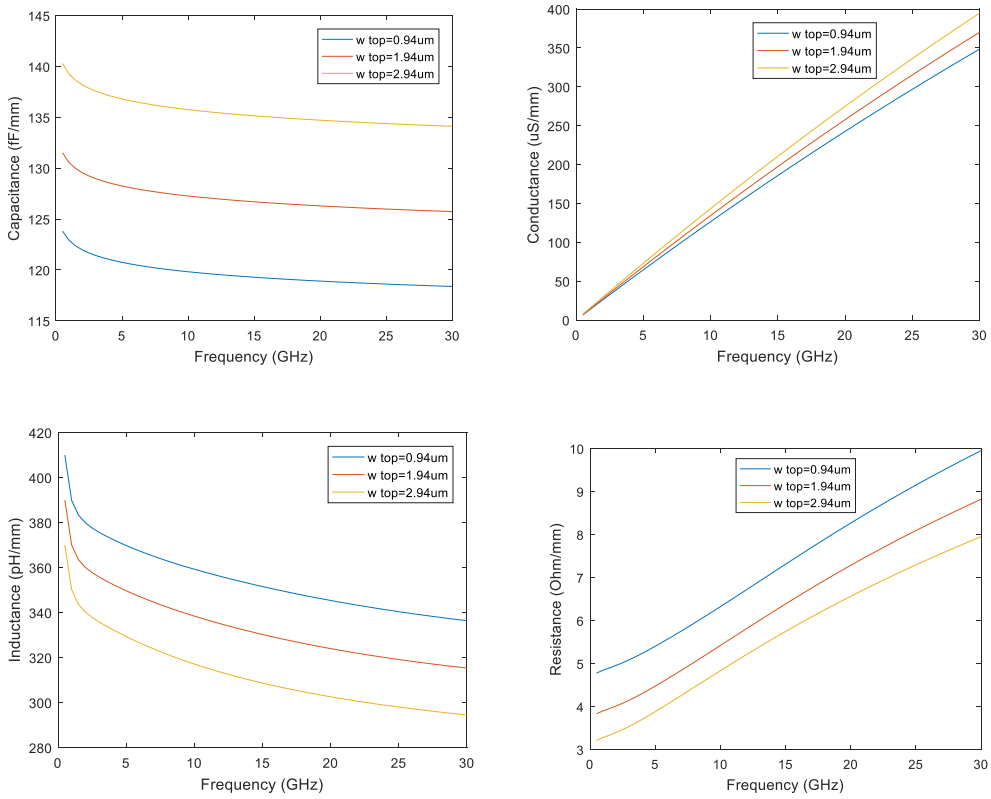


Figure 3.32: Simulated capacitance, conductance, inductance, and resistance per unit length of stripline with different copper trace width on top

Table 3.5: W_top variation and corresponding side wall taper angle for stripline

W_top variation (µm)	Side wall taper angle
2.94	90°
1.94	76°
0.94	63.4°

The cross-sectional schematics for CPW tapered side wall analysis are shown in Figure 3.33. For SAP fabricated CPW analysis, the W_bottom and Gap_bottom was fixed at 3 µm and 2.1 µm, respectively, while W_top was simulated at 0 µm, 1 µm, 2 µm, and 3 µm. For the embedded case, W_top and Gap_top was set at 3 µm and 1.475 µm,

respectively, while W_bottom was tuned at 0 µm, 1 µm, 2 µm, and 3 µm. The corresponding Gap_top for the SAP case and Gap_bottom for the embedded case satisfy the following equation

$$Gap\_top + W\_top = W\_bottom + Gap\_bottom \quad (3.5)$$

in order to keep a consistent side wall taper angle. Table 3.6 lists the corresponding side wall angles for 5 µm thick SAP fabricated CPW and 2 µm thick partially embedded CPW. The simulated RLGC of CPW by SAP method is shown in Figure 3.34, and Figure 3.35 shows the RLGC for the embedded CPW case. As expected, similar to microstrip line and stripline, narrower W_top for SAP or W_bottom for embedded results in smaller capacitance, higher inductance, and higher resistance. The conductance for SAP fabricated CPW is not affected with fixed W_bottom and Gap_bottom, the same as for the tapered SAP microstrip line case. For partially embedded CPW, the conductance decreases as the taper angle increases, along the same trend line as the partially embedded microstrip line and stripline.

Figure 3.33: Simplified tapered CPW analysis for SAP method (left) and embedded method (right)

Table 3.6: W_top and W_bottom variation and corresponding side wall taper angle for CPW

SAP method		Embedded method	
W_top variation (µm)	Side wall taper angle	W_bottom variation (µm)	Side wall taper angle
3	90°	3	90°
2	84.3°	2	104°
1	78.7°	1	116.6°
0	73.3°	0	126.9°

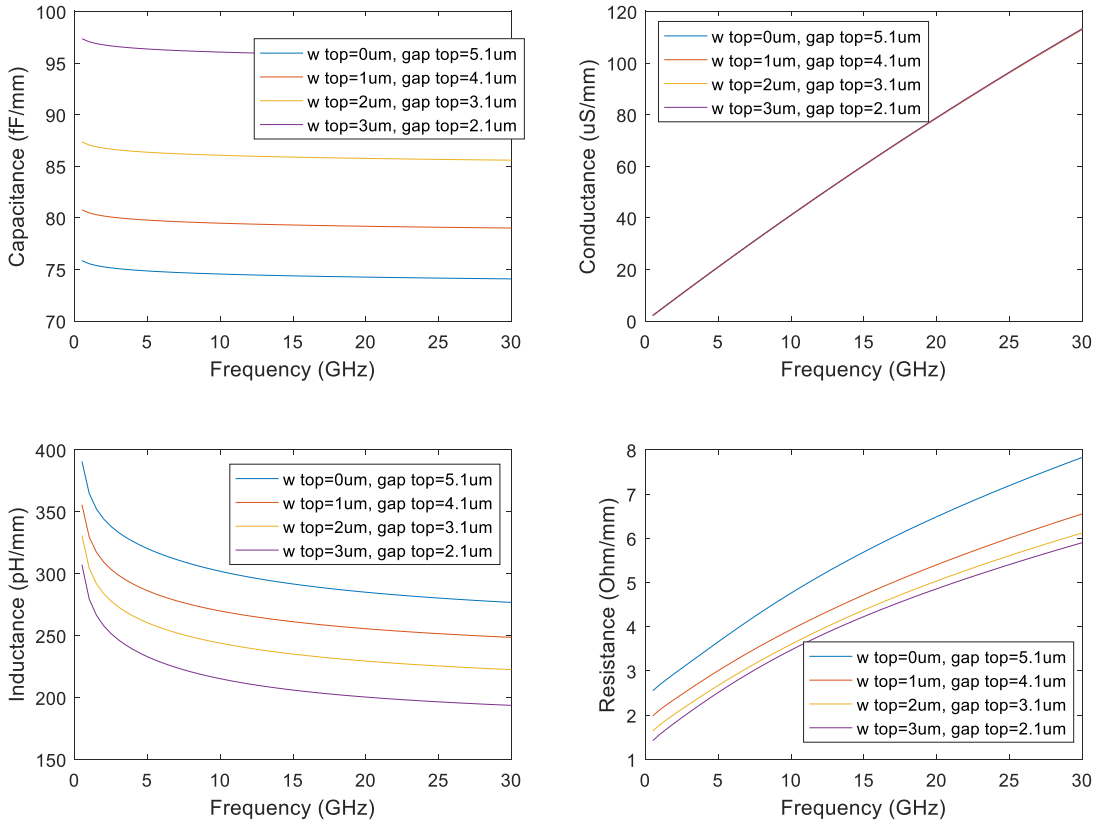


Figure 3.34: Simulated capacitance, conductance, inductance, and resistance per unit length of CPW with different copper trace top width on fixed bottom width, fabricated by SAP method

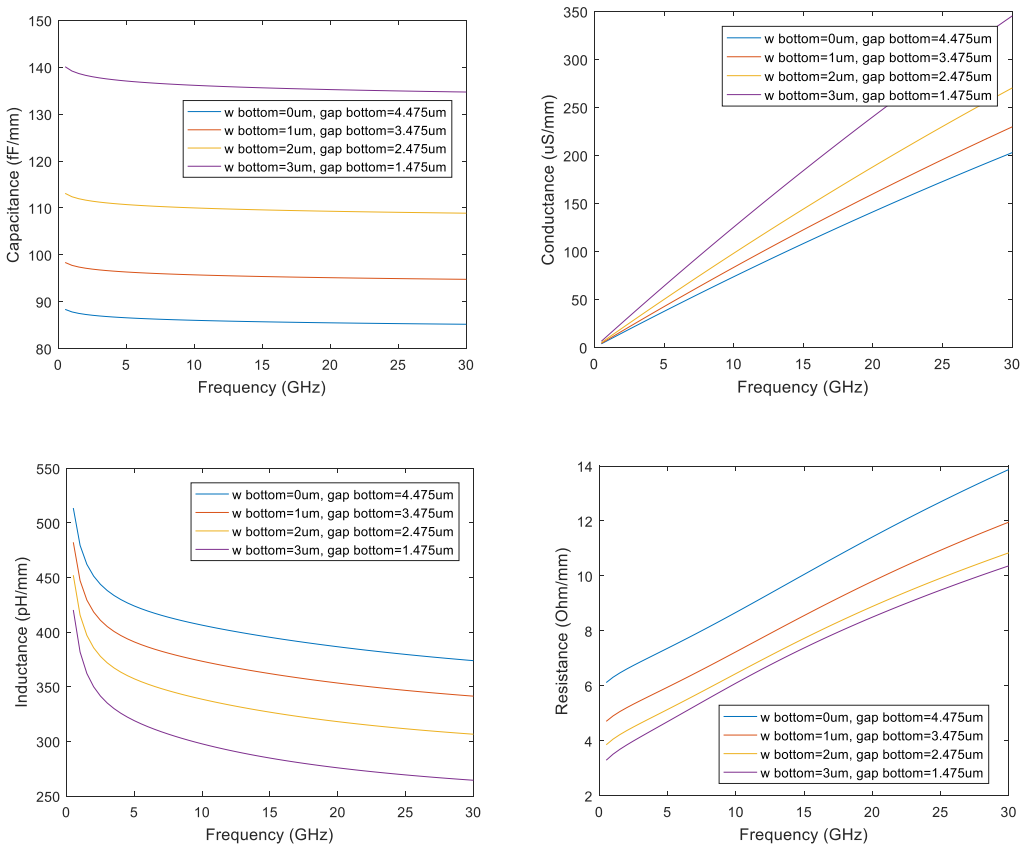


Figure 3.35: Simulated capacitance, conductance, inductance, and resistance per unit length of CPW with different copper trace bottom width on fixed top width, fabricated by SAP method

In general, for all transmission line types, tapered copper traces lead to lower capacitance, lower conductance, higher inductance, and higher resistance, with unaffected conductance for SAP fabricated CPW and microstrip line as exceptions.

If the tapered copper side wall cannot be avoided for a specific fabrication process, a design compensation factor can be applied to achieve impedance control on tapered copper traces. Using a 2D extractor model, the microstrip line with tapered side wall with same angles analyzed above were designed to achieve 50-ohm impedance, as shown in

Table 3.7. The RLGC simulation results on impedance controlled tapered microstrip line fabricated by SAP method and embedded method are shown in Figure 3.36 and Figure 3.37. According to the simulation results, the performance is quite opposite for both processes. The SAP fabricated microstrip line typically has the taper angle equal or less than 90°. When this angle decreases, all RLGC parasitic elements increase, degrading the electrical performance. However, for the embedded method, the taper angle is always equal to or larger than 90°. When this angle increases, the capacitance decreases slightly, while the other parasitic elements remain unaffected. The electrical performance improves with reduced parasitic elements for partially embedded microstrip line, at the cost of wiring density, since the width of copper trace increases with side wall taper angle to maintain impedance control. To verify this performance improvement, a 3D HFSS transmission line model with wave ports was created and simulated. The length of the partially embedded microstrip line was set at 1 mm. The impedance controlled designs for 90° and 126.9° side wall taper angles were input into the 3D model for the simulation. The simulated insertion loss and its phase are shown in Figure 3.38. According to this full-wave 3D simulation result, the impedance controlled partially embedded microstrip line has lower insertion loss and marginally smaller phase, confirming better electrical performance.

Table 3.7: Impedance controlled microstrip line design with tapered side wall

SAP method					Embedded method				
Effective dielectric thickness (μm)	Copper thickness (μm)	W_top (μm)	W_bottom (μm)	Side wall taper angle	Effective dielectric thickness (μm)	Copper thickness (μm)	W_top (μm)	W_bottom (μm)	Side wall taper angle
3	2	6.78	7.78	76°	3	2	7.25	6.25	104°
3	2	6.01	8.01	63.4°	3	2	7.79	5.79	116.6°
3	2	5.21	8.21	53.1°	3	2	8.29	5.29	126.9°

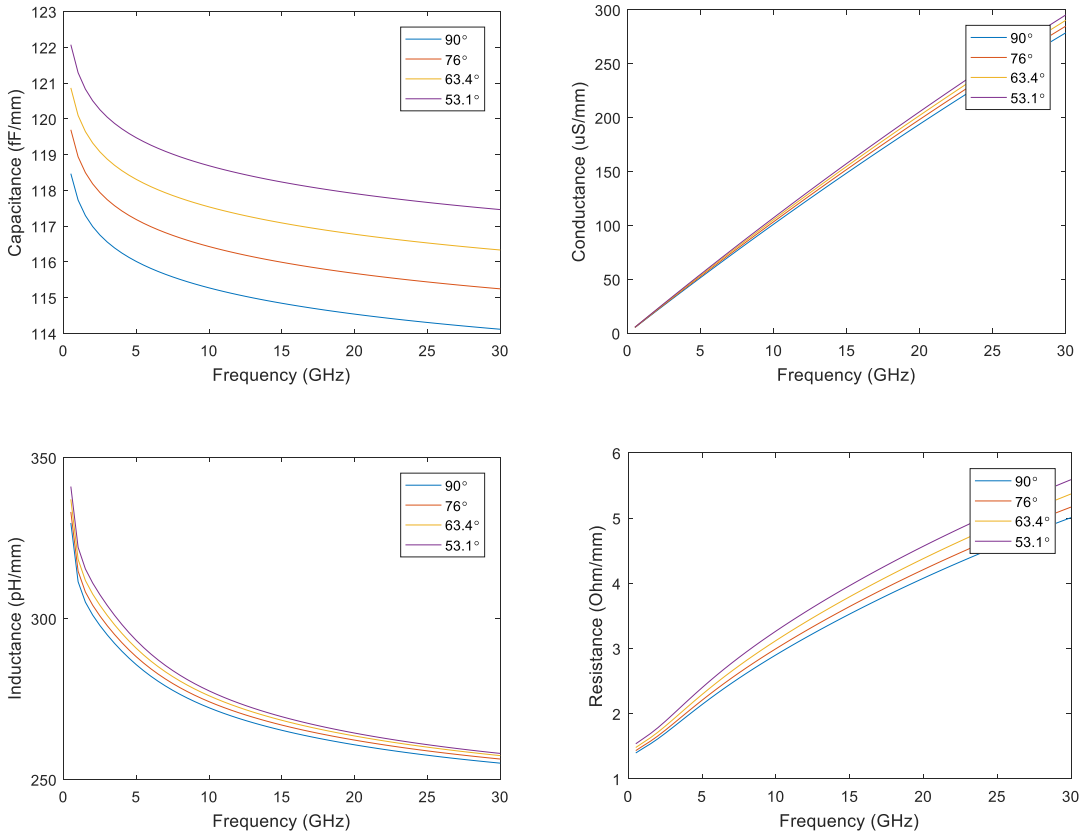


Figure 3.36: Simulated capacitance, conductance, inductance, and resistance per unit length of impedance controlled microstrip line with different side wall taper angle, fabricated by SAP method

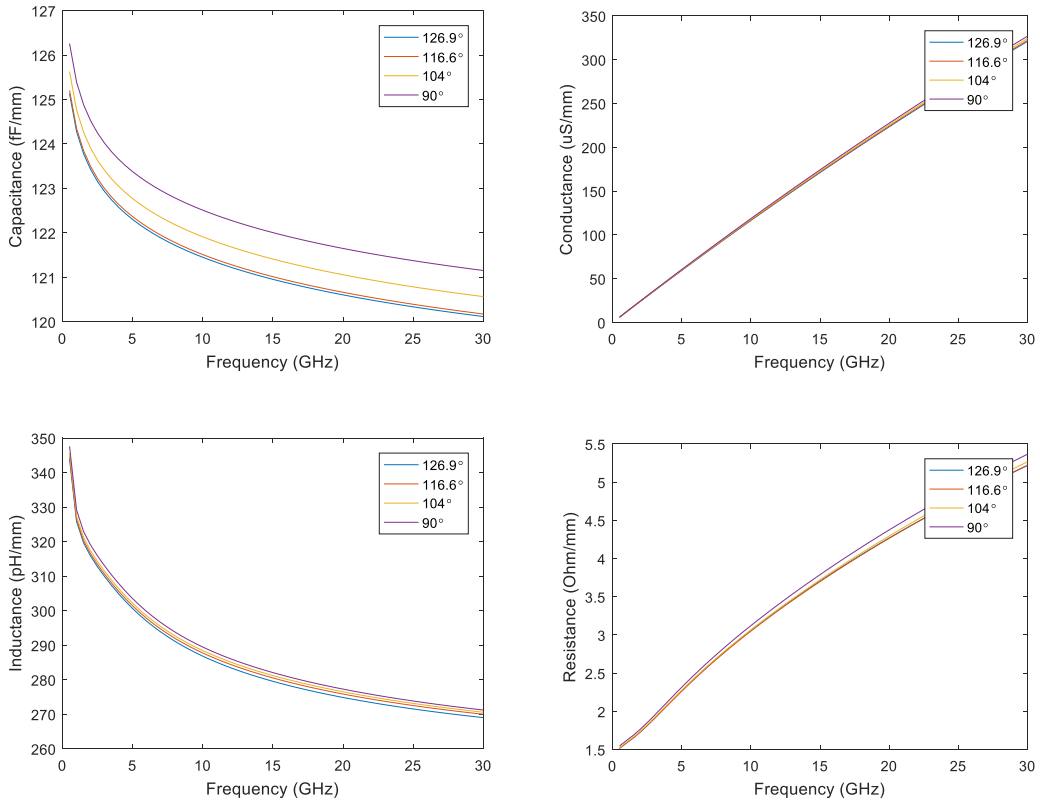


Figure 3.37: Simulated capacitance, conductance, inductance, and resistance per unit length of impedance controlled microstrip line with different side wall taper angle, fabricated by embedded method

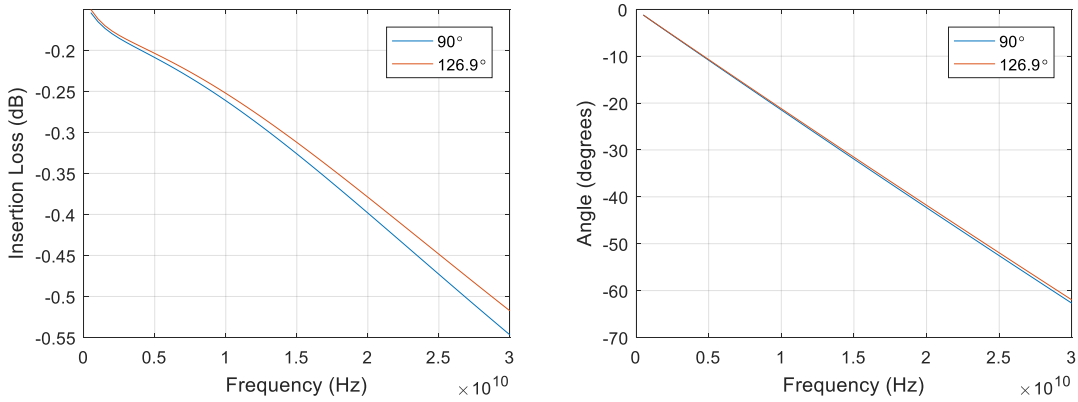


Figure 3.38: Simulated insertion loss and its phase for impedance controlled microstrip line fabricated by embedded method with different copper side wall taper angle

For impedance controlled tapered stripline, the design parameters to be analyzed are shown in Table 3.8, with no differences between the SAP model and the embedded model due to symmetry. The designed side wall taper angles are the same as the microstrip line simulation, and all designs have a characteristic impedance of 50 ohm at 5.8 GHz. The RLGC simulation results on impedance controlled tapered striplines are shown in Figure 3.39. It can be noted that vertical copper side wall design has the lowest capacitance and resistance, and consequently the lowest latency for signal transmission. The capacitance and resistance increases when the taper angle decreases, while the conductance and inductance are not affected.

Table 3.8: Impedance controlled stripline design with tapered side wall

Effective dielectric thickness (μm)	Copper thickness (μm)	W_top (μm)	W_bottom (μm)	Side wall taper angle
8	2	2.41	3.41	76°
8	2	1.82	3.82	63.4°
8	2	1.18	4.18	53.1°

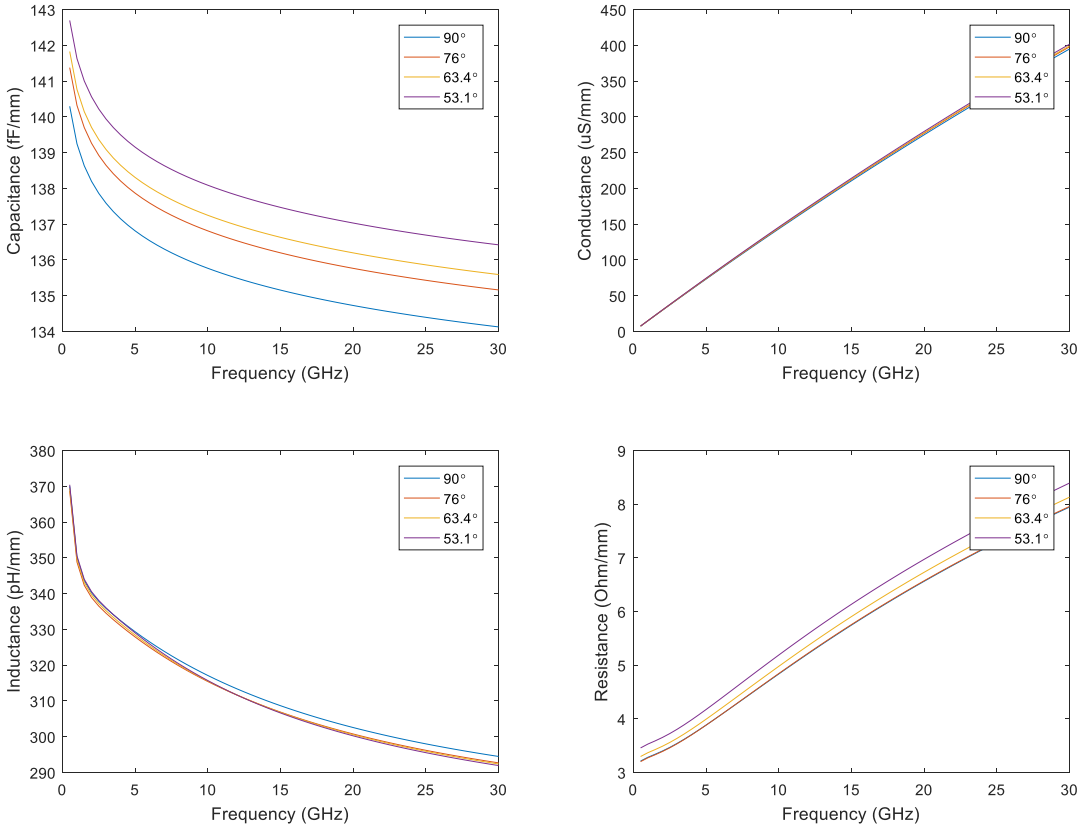


Figure 3.39: Simulated capacitance, conductance, inductance, and resistance per unit length of impedance controlled stripline with different side wall taper angle

Impedance controlled CPWs with the same set of taper angles simulated previously were also designed to achieve 50-ohm impedance at 5.8 GHz, as shown in Table 3.9. For the SAP case, the taper angle impact on RLGC was similar to that of the SAP fabricated microstrip line, as shown in Figure 3.40. When this angle decreases, all RLGC parasitic elements increase, degrading the electrical performance. Furthermore, the conductance, inductance, and resistance for CPWs are more sensitive to the taper angle than microstrip lines. For partially embedded CPW, similar results were observed,

where in the impedance controlled CPW with a non-vertical wall has higher RLGC than a non-tapered CPW, as shown in Figure 3.41.

Table 3.9: Impedance controlled CPW design with tapered side wall

SAP method						
Effective dielectric thickness (µm)	Copper thickness (µm)	W_top (µm)	W_bottom (µm)	Gap_top (µm)	Gap_bottom (µm)	Side wall taper angle
5	5	2	3	2.62	1.62	84.3°
5	5	1	3	3.2	1.2	78.7°
5	5	0	3	3.0	0.8	73.3°
Embedded method						
Effective dielectric thickness (µm)	Copper thickness (µm)	W_top (µm)	W_bottom (µm)	Gap_top (µm)	Gap_bottom (µm)	Side wall taper angle
3	2	3	2	0.913	1.913	104°
3	2	3	1	0.505	2.505	116.6°
3	2	3	0	0.23	3.23	126.9°

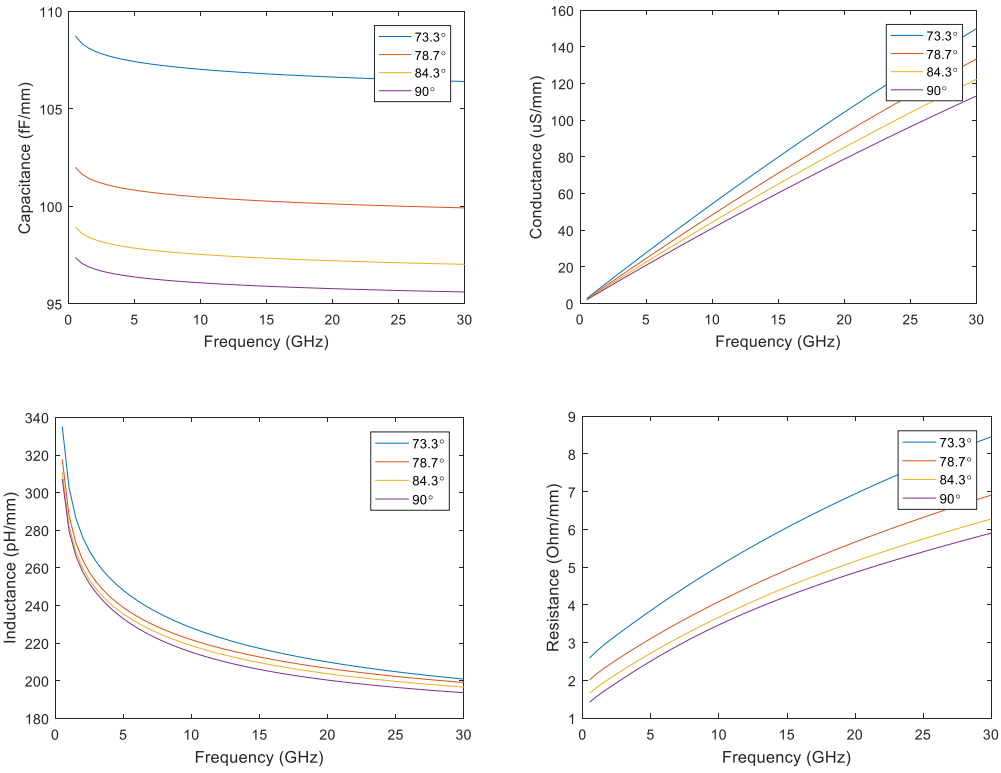


Figure 3.40: Simulated capacitance, conductance, inductance, and resistance per unit length of impedance controlled CPW with different side wall taper angle, fabricated by SAP method

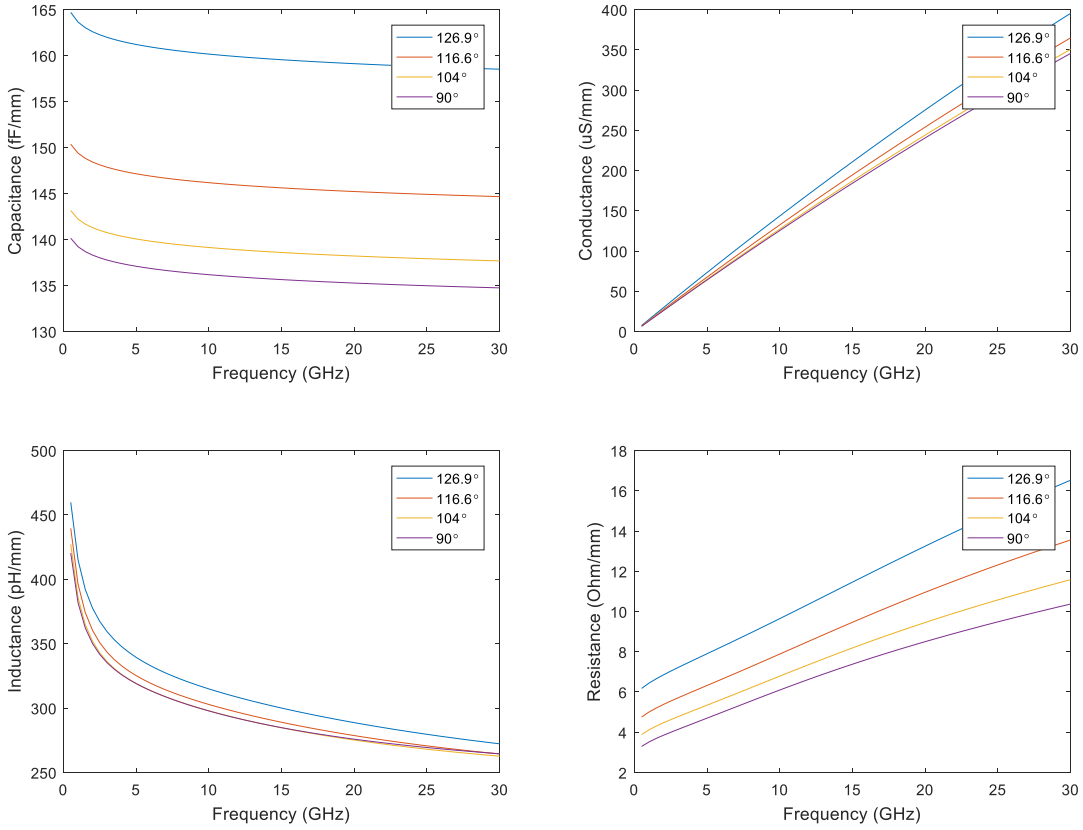


Figure 3.41: Simulated capacitance, conductance, inductance, and resistance per unit length of impedance controlled CPW with different side wall taper angle, fabricated by embedded method

In summary, even with good impedance control, the transmission lines with non-vertical side walls have worse electrical performance, with the exception of the partially embedded microstrip line. The tapered side wall slightly reduces RLGC parasitic elements for partially embedded microstrip lines at the cost of wiring density. However, the performance improvement is too subtle for wider line width with tapered side wall. Therefore, tapered copper side walls should be avoided if possible to achieve the best electrical performance and highest wiring density.

3.3.5 Copper Surface Roughness

Electrical current tends to flow along the lowest impedance path. For direct current (DC), the inductance does not affect the current distribution. However, the alternating current (AC) is affected by the inductance, and distributed towards the edge of the conductor, called the skin effect. The skin depth for a solid wire is commonly calculated by:

$$\delta_s = \sqrt{\frac{1}{\pi f \mu \sigma}} \tag{3.6}$$

where f is the AC frequency in Hz, μ is the permeability with a typical value of $4\pi*10^{-7}$ H/m, and σ is the conductivity of the conductor in S/m. The AC distribution for a microstrip line is more complicated, which can only be accurately calculated by electromagnetic simulation tools, as shown in Figure 3.12. The copper surface roughness increases the resistivity at the boundary of the copper trace due to topographic discontinuity. The effect of polymer dielectric surface roughness on AC signal propagation was simulated using Keysight ADS [35]. The microstrip line with a higher polymer-copper interface roughness showed higher insertion loss. The copper trace side wall and top surface roughness was not captured in the ADS model. However, the conductor surface roughness effect can be captured in the Ansoft 2D extractor model by using boundary conditions. The modified Hammerstad model was applied to the loss of rough copper surface to emulate the roughness effect in the 2D extractor model [36]. The model equation is as follows:

$$H_{HJ} = 1 + \left(\frac{2}{\pi}\right)(SF - 1) arctan\left[1.4\left(\frac{R_a}{\delta_s}\right)^2\right] \tag{3.6}$$

where H_{HJ} is the Hammerstad coefficient as a function of average surface roughness R_a, skin depth δ_s, and scaling factor SF. In the original Hammerstad-Jensen model, SF is equal to 2. Then,

$$\alpha_{cond,\ rough} = \alpha_{cond,smooth} H_{HJ} \tag{3.7}$$

where $\alpha_{cond,\ smooth}$ is the attenuation constant calculated for a smooth conductor. For some special cases with certain surface topographies, the SF can be tuned for better accuracy. In this study, the original scaling factor was applied in the 2D model. The surface roughness boundary condition was added to the previous 2D extractor model, and the solve option for signal and reference conductors was changed to "solve on boundary" in order to enable the added surface roughness boundary condition. The conductor thickness for "solve on boundary" was set to be the ratio of conductor area over its perimeter for accurate simulation results. Changing the solve option slightly affects the optimal design parameters to achieve 50-ohm impedance for microstrip line, with the width of the trace reduced to 7.1 μm for SAP microstrip line, and 6.23 μm for partially embedded microstrip line, which were applied for the surface roughness analysis. For the SAP method, the surface roughness on the bottom boundary of the copper structure is caused by the desmear process, while the vertical and top boundary roughness is induced by the seed layer etch process. For the embedded case, the copper trace vertical and bottom boundary roughness is the same as trench surface roughness during trench formation, and the top boundary roughness is determined by surface planarization process. The surface roughness caused by different process steps at different locations is shown in Figure 3.42. To simplify the analysis, four scenarios for the SAP method were considered as listed in

Table 3.10, and an additional four scenarios for the embedded method were considered as listed in Table 3.11. These scenarios were also applied for stripline and CPW analysis.

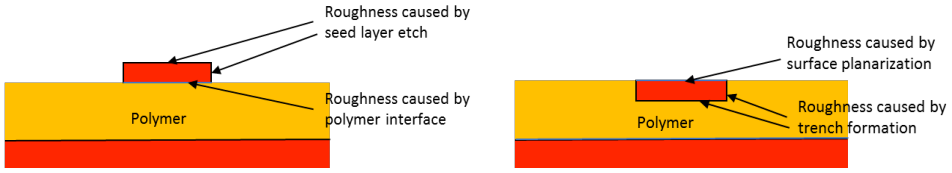


Figure 3.42: Copper surface roughness caused by different mechanisms

Table 3.10: Four surface roughness scenarios considered for SAP method

Scenario 1: No desmear on polymer, smooth copper surface	Roughness on bottom surface	0.014 µm
	Roughness on side wall and top surface	0.014 µm
Scenario 2: Desmear on polymer, copper surface roughness same as polymer	Roughness on bottom surface	0.1 µm
	Roughness on side wall and top surface	0.1 µm
Scenario 3: Desmear on polymer, rough copper surface and side wall	Roughness on bottom surface	0.1 µm
	Roughness on side wall and top surface	0.5 µm
Scenario 4: Desmear on polymer, very rough copper surface and side wall	Roughness on bottom surface	0.1 µm
	Roughness on side wall and top surface	1 µm

Table 3.11: Four surface roughness scenarios considered for embedded method

Scenario 1: Smooth polymer trench and copper surface	Roughness on side wall and bottom surface	0.014 µm
	Roughness on top surface	0.014 µm
Scenario 2: Increased polymer trench roughness and smooth copper top boundary	Roughness on side wall and bottom surface	0.1 µm
	Roughness on top surface	0.014 µm
Scenario 3: Rough polymer trench and smooth copper top boundary	Roughness on side wall and bottom surface	0.5 µm
	Roughness on top surface	0.014 µm
Scenario 4: Desmear on polymer, very rough copper surface and side wall	Roughness on side wall and bottom surface	1 µm
	Roughness on top surface	0.014 µm

The simulated RLGC for SAP microstrip line is shown in Figure 3.43. According to the simulations, a rougher copper surface has higher inductance and resistance, while the capacitance and conductance are not affected by surface roughness. Typically, the fabricated microstrip lines with optimized SAP method falls in Scenario 2, which has almost identical performance compared to microstrip line with very smooth copper in Scenario 1. Therefore, according to the RLGC simulation for microstrip line by SAP method with conductor surface roughness variations, the electrical performance influenced by copper surface roughness effect is the least significant among all four process variations.

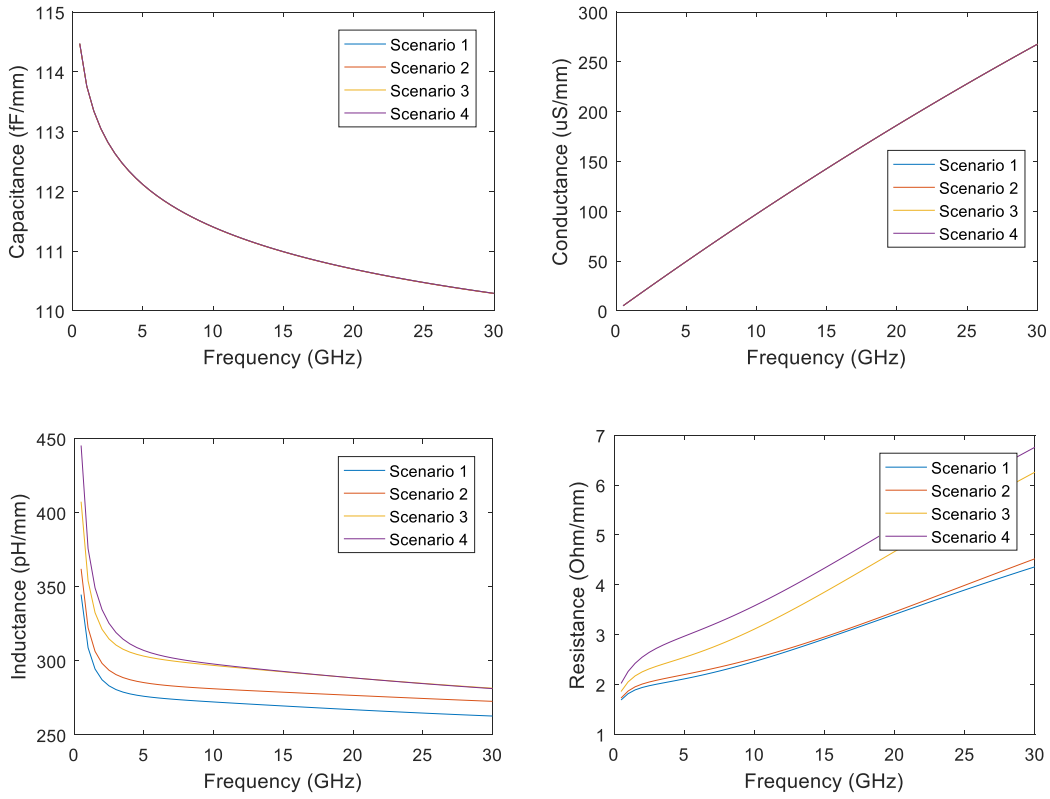


Figure 3.43: Simulated capacitance, conductance, inductance, and resistance per unit length of microstrip line with different surface roughness scenarios, fabricated by SAP method

Figure 3.44 shows the simulated RLGC for a partially embedded microstrip line. The impact due to surface roughness is close to the SAP fabricated microstrip line model. The capacitance and conductance are not affected by rough copper surface, but the inductance and resistance increase with copper roughness. Depending on the polymer type and trench formation method, the copper surface roughness can be as high as in Scenario 3. Even though, the impact of the copper surface roughness for partially embedded microstrip line is still the least significant among all four process variations.

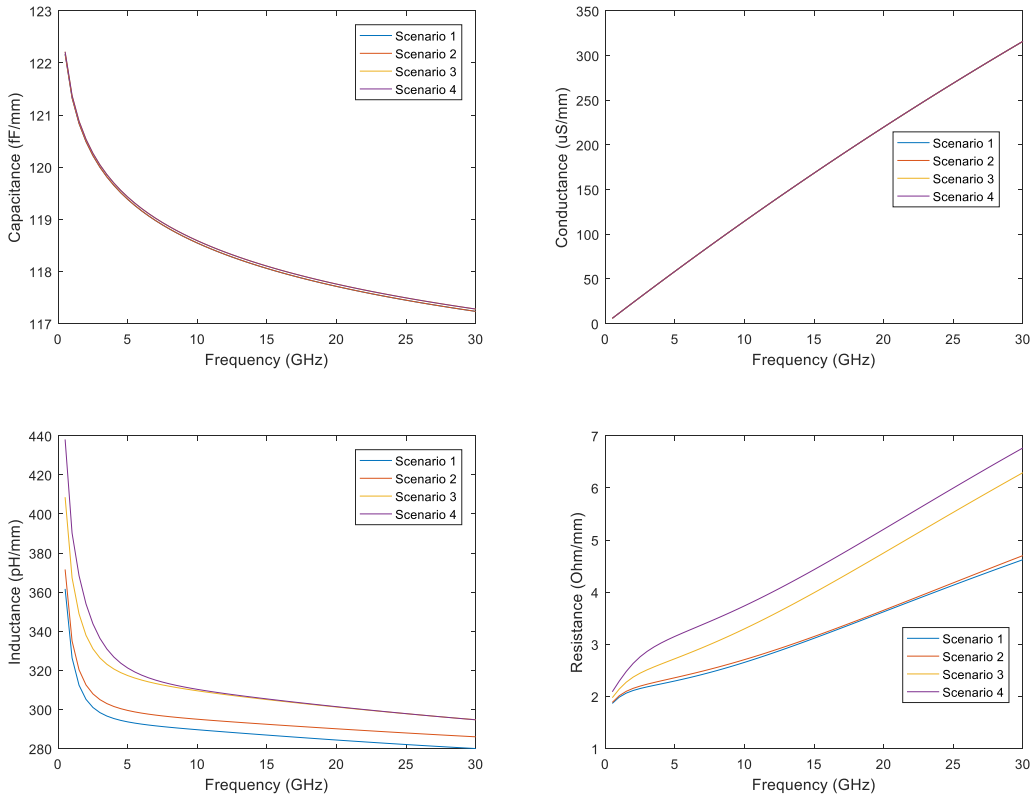


Figure 3.44: Simulated capacitance, conductance, inductance, and resistance per unit length of microstrip line with different surface roughness scenarios, fabricated by embedded method

The copper surface roughness impact for stripline analysis was carried out in two different 2D models for the SAP and embedded methods, due to different scenario setups. With “solve on boundary” setting, the impedance controlled stripline with 5 µm thick ABF dielectric layer had a line width of 2.65 µm. Figure 3.45 shows the result of RLGC simulations for stripline with the four SAP surface roughness scenarios. The embedded case results are shown in Figure 3.46. According to the simulations, the capacitance and conductance of the stripline are not affected by the copper surface roughness, similar to the microstrip line. The inductance and resistance are higher for the rougher copper scenarios, as expected for both SAP and embedded methods.

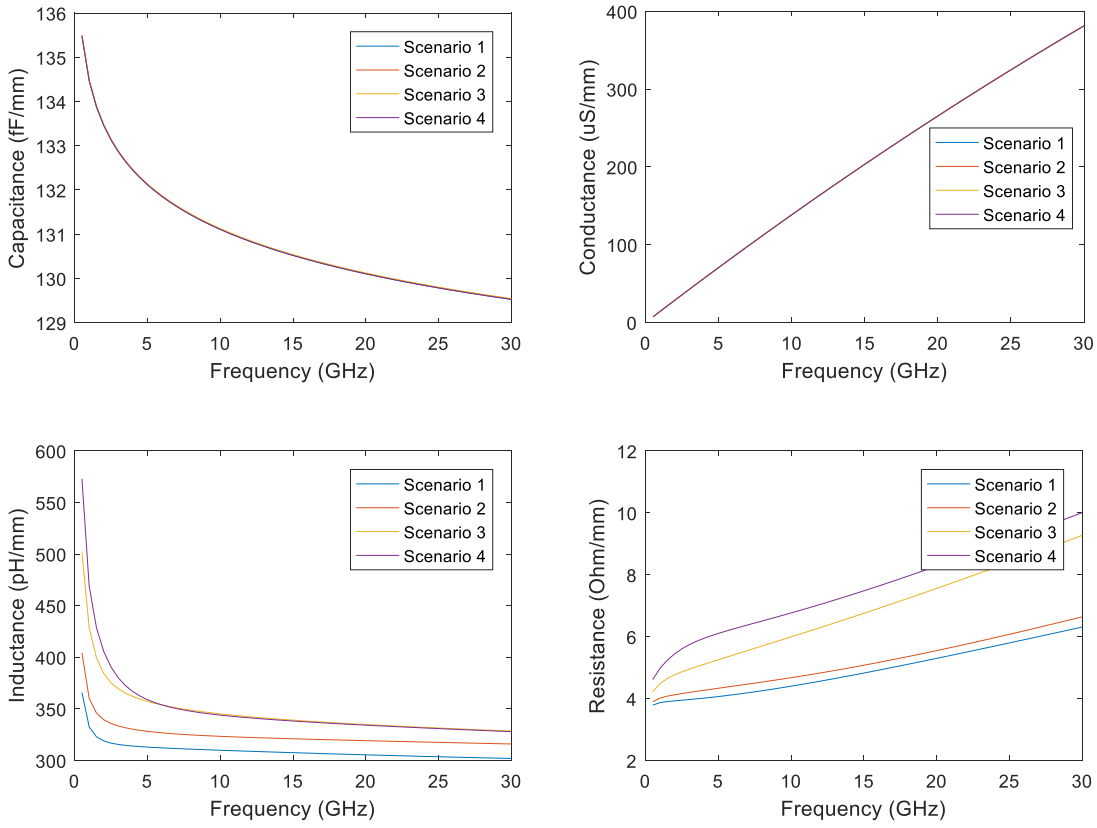


Figure 3.45: Simulated capacitance, conductance, inductance, and resistance per unit length of stripline with different surface roughness scenarios, fabricated by SAP method

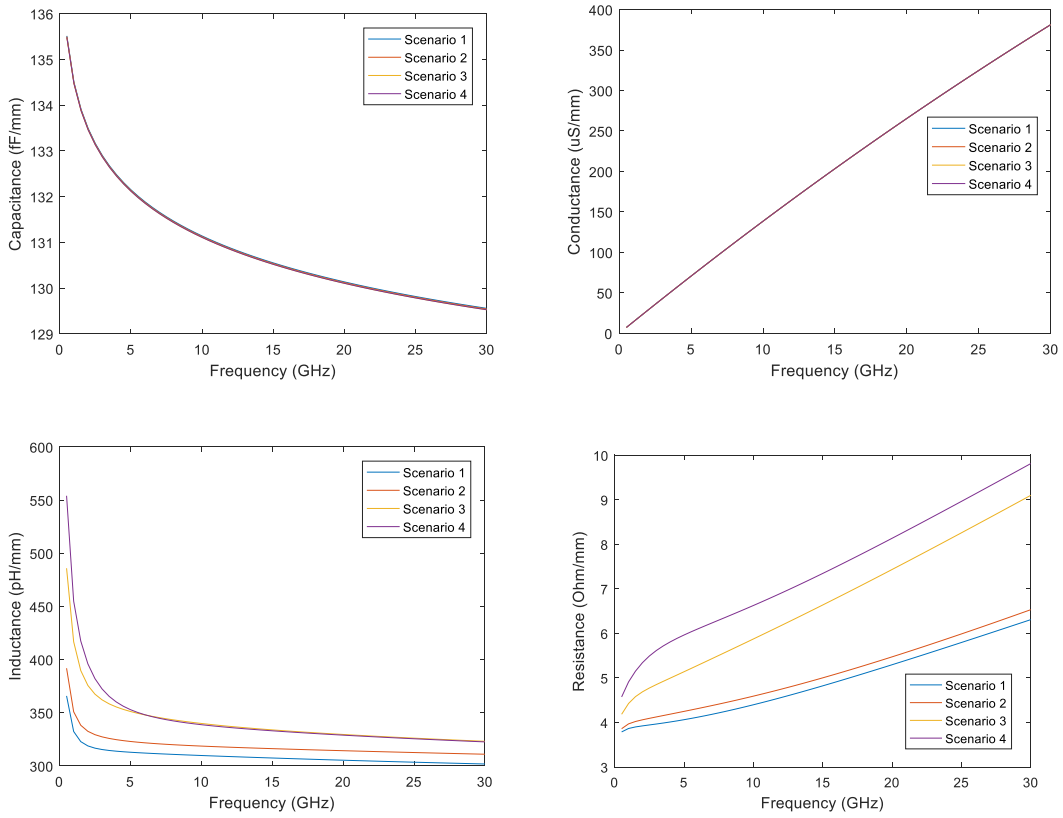


Figure 3.46: Simulated capacitance, conductance, inductance, and resistance per unit length of stripline with different surface roughness scenarios, fabricated by embedded method

The copper surface roughness impact analysis was also performed for CPW lines with the two fabrication methods. The impedance controlled design for CPW lines fabricated by the SAP method was updated for 5 µm thick ABF, and the line width was 3 µm with a gap of 2.26 µm. The partially embedded CPW design was also updated to have line thickness of 2 µm, width of 3 µm, and gap of 1.688 µm. The simulation results (Figure 3.47 for SAP and Figure 3.48 for embedded) showed a trend similar to that of the microstrip line and stripline cases. Only the inductance and resistance were affected by the copper surface roughness.

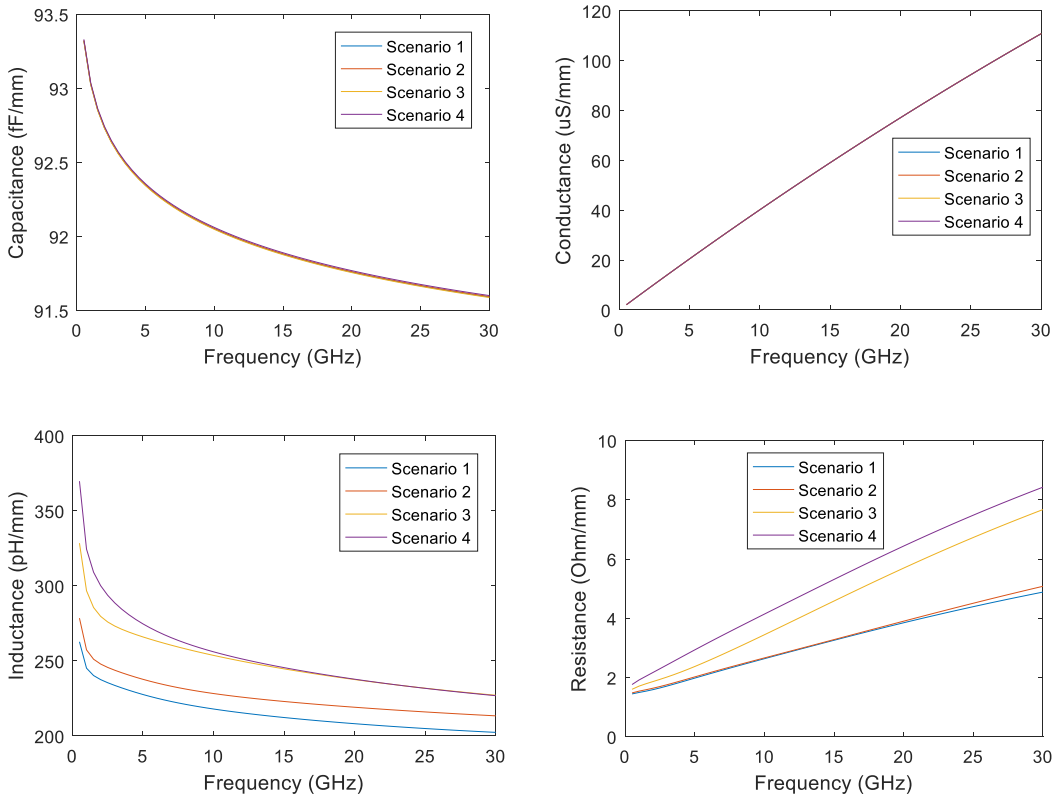


Figure 3.47: Simulated capacitance, conductance, inductance, and resistance per unit length of CPW with different surface roughness scenarios, fabricated by SAP method

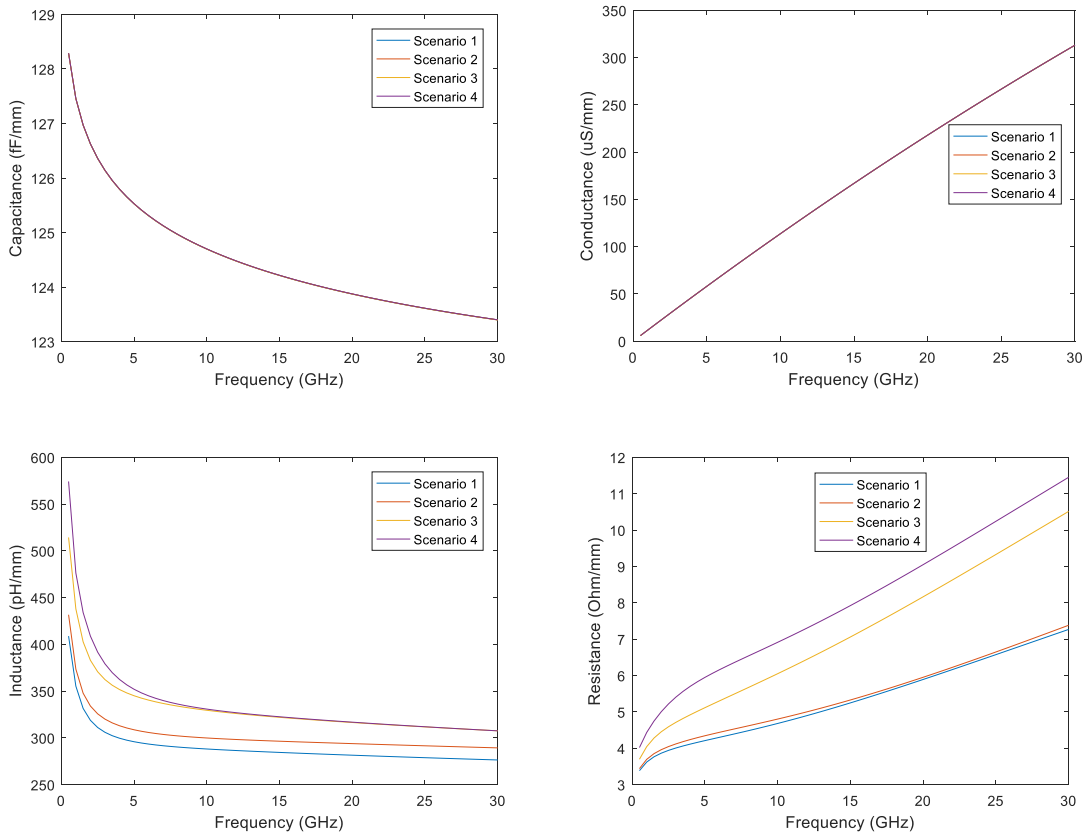


Figure 3.48: Simulated capacitance, conductance, inductance, and resistance per unit length of CPW with different surface roughness scenarios, fabricated by embedded method

To summarize this section, the copper surface roughness added to the 2D model increases the inductance and resistance across all types of transmission lines. However, the performance impact is the least significant among the four process variations analyzed in this chapter.

3.4 Characteristic Impedance Sensitivity of Process Variations

In the previous section, the parasitic RLGC of three types of transmission lines fabricated by two different methods with four types of process variations were simulated by 2D extractor modeling. The characteristic impedance of the transmission line can be calculated by:

$$Z_0 = \sqrt{\frac{R+j\omega L}{G+j\omega C}} \tag{3.8}$$

where R is the resistance per unit length, L is the inductance per unit length, G is the conductance per unit length, C is the capacitance per unit length, and ω is the angular frequency. In this section, the characteristic impedance sensitivity of four types of process variations is analyzed to arrive at a set of design rules based on the impedance tolerance specifications for different applications.

3.4.1 Copper Trace Width Variations

For all transmission line types, narrower signal traces lead to lower capacitance, lower conductance, higher inductance, and higher resistance, resulting in higher characteristic impedance, and vice versa for wider signal traces, as analyzed in previous section. This section discusses a more quantitative analysis of line width variation impacts for each of the transmission line types. The characteristic impedance of microstrip lines fabricated by SAP and embedded methods at 5.8 GHz, subjected to width variations were calculated, as shown in Figure 3.49. For a certain width change, independent of the original width, the impedance of a finer microstrip line is more sensitive to width variations. The calculated microstrip line width for different impedance

tolerance targets is listed in Table 3.12. According to these results, for a given impedance tolerance, the absolute width tolerance for finer microstrip line is smaller, but the percentage relative tolerance based on the impedance controlled design is higher. Thus, the impedance is more sensitive when the width is narrower than designed.

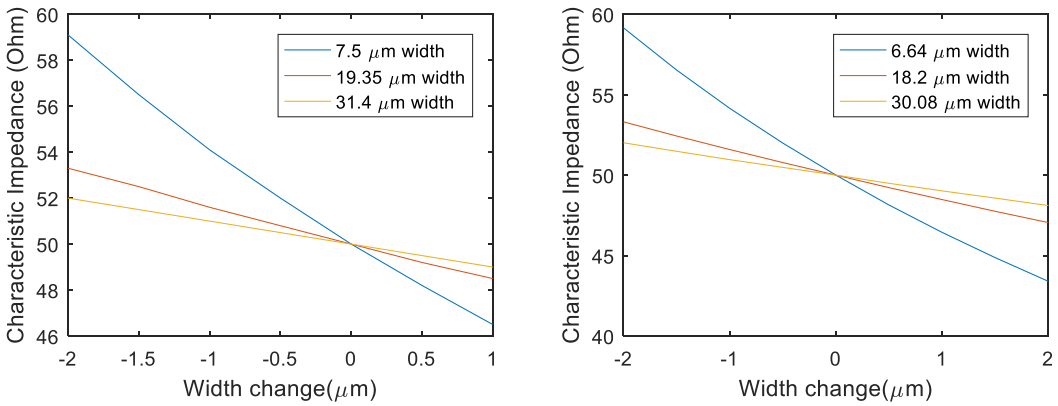


Figure 3.49: Simulated capacitance, conductance, inductance, and resistance per unit length of CPW with different surface roughness scenarios, fabricated by embedded method

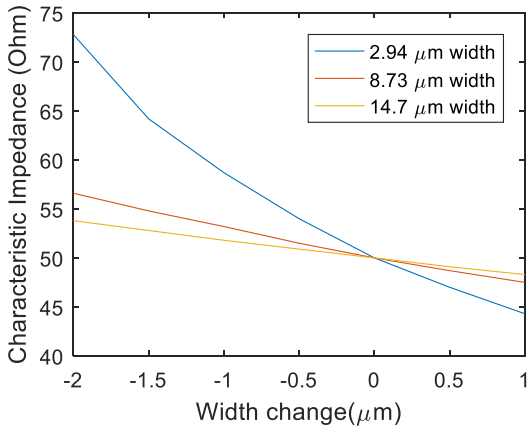


Figure 3.50: Characteristic impedance of microstrip line with trace width variation for 2 µm copper thickness

Table 3.12: Calculated microstrip line width target for different impedance tolerance

SAP method							
		5 µm ABF		10 µm ABF		15 µm ABF	
Characteristic impedance (Ohm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change
50	0	7.5	0	19.35	0	31.4	0
50.5	+1%	7.368	-1.76%	19.02	-1.71%	30.88	-1.66%
52.5	+5%	6.88	-8.27%	17.81	-7.96%	28.94	-7.83%
55	+10%	6.317	-15.77%	16.451	-14.98%	26.75	-14.81%
49.5	-1%	7.63	+1.73%	19.67	+1.65%	31.9	+1.59%
47.5	-5%	8.19	+9.2%	21.05	+8.79%	34.09	+8.57%
45	-10%	8.961	+19.48%	22.95	+18.6%	37.11	+18.18%
Embedded method							
		5 µm ABF		10 µm ABF		15 µm ABF	
Characteristic impedance (Ohm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change
50	0	6.64	0	18.2	0	30.08	0
50.5	+1%	6.509	-1.97%	17.87	-1.81%	29.56	-1.73%
52.5	+5%	6.016	-9.4%	16.67	-8.41%	27.61	-8.21%
55	+10%	5.459	-17.79%	15.29	-15.99%	25.41	-15.53%
49.5	-1%	6.77	+1.96%	18.52	+1.76%	30.57	+1.63%
47.5	-5%	7.261	+9.35%	19.87	+9.18%	32.77	+8.94%
45	-10%	8.099	+21.97%	21.78	+19.67%	35.77	+18.92%

Similar to the previous stripline analysis, the two fabrication methods share the same model. The calculated characteristic impedance versus the trace width change plot is shown in Figure 3.50. All the calculations were based on the impedance controlled design of striplines in Section 3.1.2, with a copper thickness of 2 µm. The width tolerance for different impedance tolerances were also calculated, as shown in Table 3.13. The results are similar to the microstrip line outcomes, wherein the absolute width tolerance for a given impedance control target is smaller, but the percentage relative tolerance is higher, and the impedance control requirement for narrower traces is more stringent than for wider traces.

Table 3.13: Calculated stripline width target for different impedance tolerance

		5 μm ABF		10 μm ABF		15 μm ABF	
Characteristic impedance (Ohm)	Percentage change	Trace width (μm)	Percentage change	Trace width (μm)	Percentage change	Trace width (μm)	Percentage change
50	0	2.94	0	8.73	0	14.7	0
50.5	+1%	2.865	-2.55%	8.557	-1.98%	14.457	-1.65%
52.5	+5%	2.592	-11.8%	7.893	-9.59%	13.38	-8.98%
55	+10%	2.279	-22.48%	7.138	-18.24%	12.172	-17.2%
49.5	-1%	3.011	+2.41%	8.911	+2.07%	15.002	+2.05%
47.5	-5%	3.326	+13.1%	9.655	+10.6%	16.2	+10.2%
45	-10%	3.751	+27.59%	10.69	+22.45%	17.844	+21.39%

The SAP fabricated CPW and partially embedded CPW were analyzed as well based on the impedance controlled design in Section 3.1.3 for 5 μm ABF thickness only, as shown in Figure 3.51. When the signal line width changes due to different process variations, the ground trace width changes accordingly, resulting in the constant sum of signal width and gap, same as in the RLGC analysis. Table 3.14 shows the calculated width targets for different impedance tolerances. The absolute width tolerance for a given impedance control target is smaller, but the percentage relative tolerance is higher, similar to the previous results for microstrip and stripline. However, the impedance is a bit more sensitive when the width is wider than designed, for the gap between signal and ground traces is narrower.

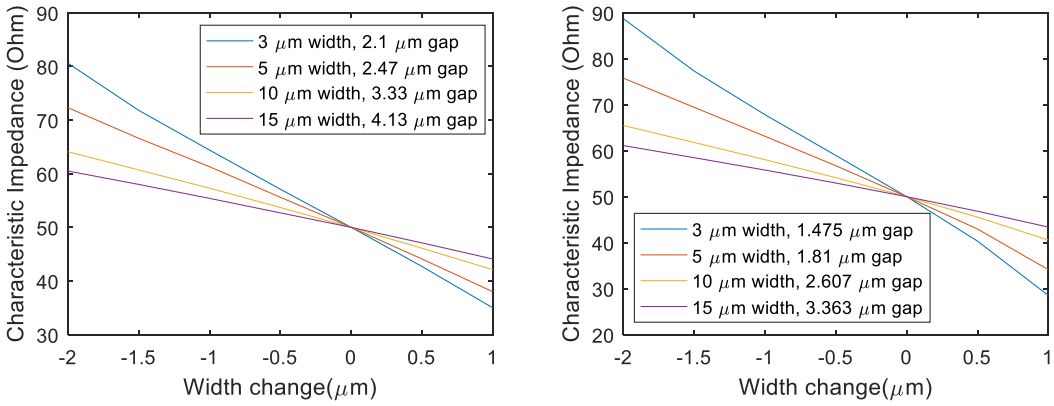


Figure 3.51: Characteristic impedance of CPW with trace width variation for SAP method with 5 µm thick copper (left) and embedded method with 2 µm thick copper (right)

Table 3.14: Calculated CPW width target for different impedance tolerance

SAP method, 5 µm thick copper, 5 µm ABF									
		3 µm width, 2.1 µm gap		5 µm width, 2.47 µm gap		10 µm width, 3.33 µm gap		15 µm width, 4.13 µm gap	
Characteristic impedance (Ohm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change
50	0	3	0	5	0	10	0	15	0
50.5	+1%	2.964	-1.2%	4.955	-0.9%	9.928	-0.72%	14.909	-0.607%
52.5	+5%	2.82	-6%	4.78	-4.4%	9.66	-3.4%	14.54	-3.07%
55	+10%	2.646	-11.8%	4.556	-8.88%	9.312	-6.88%	14.073	-6.18%
49.5	-1%	3.033	+1.1%	5.043	+0.86%	10.063	+0.63%	15.088	+0.587%
47.5	-5%	3.17	+5.67%	5.216	+4.32%	10.32	+3.2%	15.43	+2.87%
45	-10%	3.344	+11.47%	5.428	+8.56%	10.638	+6.38%	15.851	+5.67%
Embedded method, 2 µm thick copper, 5 µm ABF									
		3 µm width, 1.475 µm gap		5 µm width,1.81 µm gap		10 µm width, 2.607 µm gap		15 µm width, 3.363 µm gap	
Characteristic impedance (Ohm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change	Trace width (µm)	Percentage change
50	0	3	0	5	0	10	0	15	0
50.5	+1%	2.973	-0.9%	4.964	-0.72%	9.943	-0.57%	14.919	-0.54%
52.5	+5%	2.863	-4.57%	4.818	-3.64%	9.7	-3%	14.582	-2.79%
55	+10%	2.723	-9.23%	4.631	-7.38%	9.392	-6.08%	14.143	-5.71%
49.5	-1%	3.027	+0.9%	5.037	+0.74%	10.06	+0.6%	15.08	+0.533%
47.5	-5%	3.136	+4.53%	5.178	+3.56%	10.287	+2.87%	15.397	+2.65%
45	-10%	3.266	+8.87%	5.348	+6.96%	10.558	+5.58%	15.774	+5.16%

In summary, for all transmission line types, narrower than designed signal traces have a higher impedance, and vice versa. The impedance is more sensitive for narrower microstrip line and stripline. The impedance of CPW is more sensitive to the gap size than the signal trace width.

3.4.2 Copper Thickness Variations

According to the RLGC analysis for all transmission line types, thinner traces result in lower capacitance, lower conductance, higher inductance, and higher resistance, leading to higher characteristic impedance. The detailed analysis of copper thickness variation impact on impedance control for each transmission line type is described in this section. Figure 3.52 shows the calculated characteristic impedance of microstrip lines fabricated by SAP and embedded methods at 5.8 GHz with different copper thicknesses for a fixed width. In addition, the thickness tolerance for different impedance targets were calculated, as shown in Table 3.15. It needs to be noted that the copper thickness affects the effective dielectric thickness as an assumption in the previous RLGC analysis, and also applied in this analysis. The results indicate that for a given impedance tolerance, the absolute thickness tolerance for finer microstrip line is smaller, as well as the percentage relative tolerance based on the impedance controlled design. The impedance sensitivity is almost linear with copper thickness for the simulated range.

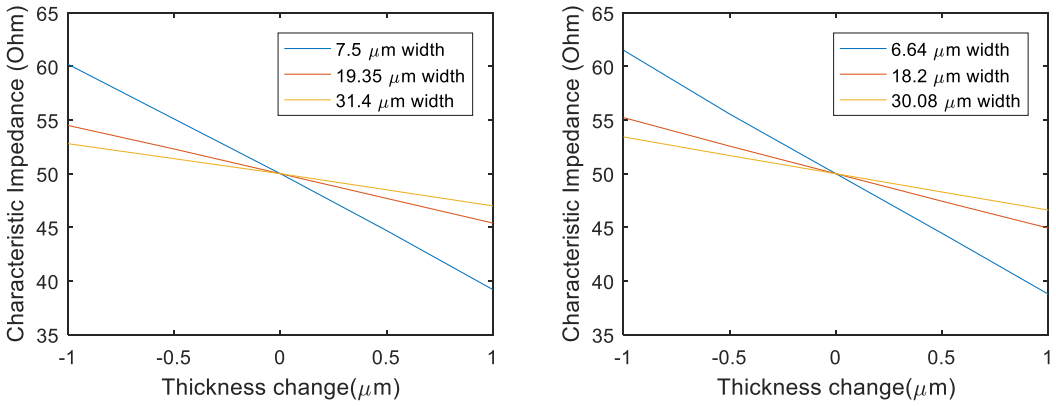


Figure 3.52: Characteristic impedance of microstrip line with copper thickness variation on 2 µm original copper thickness, fabricated by SAP method (left) and embedded method (right)

Table 3.15: Calculated microstrip line copper thickness target for different impedance tolerance

SAP method							
		5 µm ABF, 7.5 µm line width		10 µm ABF, 19.35 µm line width		15 µm ABF, 31.4 µm line width	
Characteristic impedance (Ohm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change
50	0	2	0	2	0	2	0
50.5	+1%	1.952	-2.4%	1.886	-5.7%	1.822	-8.9%
52.5	+5%	1.76	-12%	1.44	-28%	1.13	-43.5%
55	+10%	1.507	-24.65%	0.888	-55.6%	0.416	-79.2%
49.5	-1%	2.048	+2.4%	2.107	+5.35%	2.162	+8.1%
47.5	-5%	2.24	+12%	2.55	+27.5%	2.84	+42%
45	-10%	2.473	+23.65%	3.091	+54.55%	3.668	+83.4%
Embedded method							
		5 µm ABF, 6.64 µm line width		10 µm ABF, 18.2 µm line width		15 µm ABF, 30.08 µm line width	
Characteristic impedance (Ohm)	Percentage change	Copper thickness (µm)	Copper thickness (µm)	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change
50	0	2	0	2	0	2	0
50.5	+1%	1.954	-2.3%	1.9	-5%	1.847	-7.65%
52.5	+5%	1.774	-11.3%	1.514	-24.3%	1.26	-37%
55	+10%	1.548	-22.6%	1.042	-47.9%	0.6071	-69.65%
49.5	-1%	2.044	+2.2%	2.09	+4.5%	2.139	+6.95%
47.5	-5%	2.225	+11.25%	2.48	+24%	2.734	+36.7%
45	-10%	2.449	+22.45%	2.986	+49.3%	3.486	+74.3%

Copper thickness variation for striplines also affects the effective dielectric thickness. Figure 3.53 shows the calculated impedance of striplines with copper thickness variance relative to the original thickness, and Table 3.16 lists the thickness tolerance for different impedance targets. The simulation results show the same trend as microstrip line, with the absolute thickness tolerance and the percentage relative tolerance being smaller for a certain impedance tolerance for finer stripline structures. The impedance sensitivity is slightly larger when the thickness is smaller than the designed value.

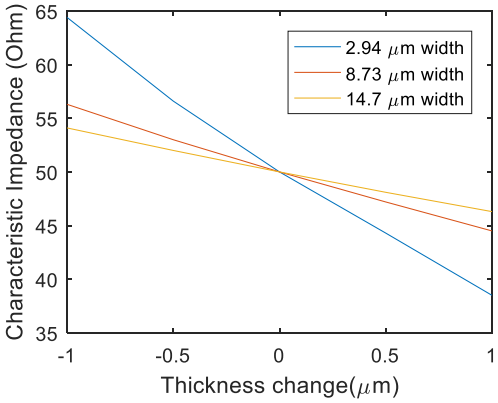


Figure 3.53: Characteristic impedance of stripline with copper thickness variation on 2 µm original copper thickness

Table 3.16: Calculated stripline copper thickness target for different impedance tolerance

		5 µm ABF, 2.94 µm line width		10 µm ABF, 8.73 µm line width		15 µm ABF, 14.7 µm line width	
Characteristic impedance (Ohm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change
50	0	2	0	2	0	2	0
50.5	+1%	1.958	-2.1%	1.913	-4.35%	1.878	-6.1%
52.5	+5%	1.82	-9%	1.59	-20.5%	1.38	-31%
55	+10%	1.599	-20.05%	1.173	-41.35%	0.812	-59.4%
49.5	-1%	2.04	+2%	2.088	+4.4%	2.137	+6.85%
47.5	-5%	2.23	+11.5%	2.46	+23%	2.67	+33.5%
45	-10%	2.42	+21%	2.898	+44.9%	3.356	+67.8%

The copper thickness change has no effect on the effective dielectric thickness for SAP fabricated CPWs, but does have an impact for the partially embedded CPWs. The impedance of CPW lines with copper thickness variations was calculated by 2D extractor modeling at 5.8 GHz, based on the impedance controlled design in the previous section for both fabrication methods, as shown in Figure 3.54. The SAP fabricated CPW lines had the original copper thickness of 5 µm instead of 2 µm for all other types of transmission lines including partially embedded CPW. The thickness tolerance for different impedance targets were calculated, as shown in Table 3.17. According to the simulation results, the absolute thickness tolerance as well as the percentage relative tolerance is smaller for a certain impedance tolerance on finer CPW. The impedance is more sensitive when the thickness is thinner than designed for both fabrication methods.

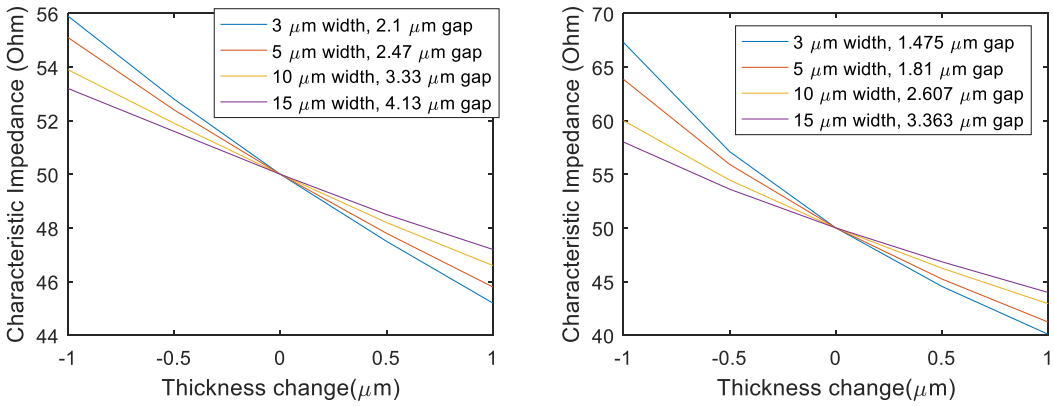


Figure 3.54: Characteristic impedance of CPW with copper thickness variation for SAP method with 5 µm original thick copper (left) and embedded method with 2 µm original thick copper (right)

Table 3.17: Calculated CPW copper thickness target for different impedance tolerance

SAP method, 5 µm thick copper, 5 µm ABF									
		3 µm width, 2.1 µm gap		5 µm width, 2.47 µm gap		10 µm width, 3.33 µm gap		15 µm width, 4.13 µm gap	
Characteristic impedance (Ohm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change
50	0	5	0	5	0	5	0	5	0
50.5	+1%	4.902	-1.96%	4.891	-2.18%	4.855	-2.9%	4.83	-3.4%
52.5	+5%	4.55	-9%	4.49	-10.2%	4.34	-13.2%	4.21	-15.8%
55	+10%	4.14	-17.2%	4.02	-19.6%	3.738	-25.24%	3.484	-30.32%
49.5	-1%	5.09	+1.8%	5.106	+2.12%	5.132	+2.64%	5.16	+3.2%
47.5	-5%	5.49	+9.8%	5.56	+11.2%	5.72	+14.4%	5.87	+17.4%
45	-10%	6.042	+20.84%	6.196	+23.92%	6.529	+30.58%	6.843	+36.86%
Embedded method, 2 µm thick copper, 5 µm ABF									
		3 µm width, 1.475 µm gap		5 µm width,1.81 µm gap		10 µm width, 2.607 µm gap		15 µm width, 3.363 µm gap	
Characteristic impedance (Ohm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change	Copper thickness (µm)	Percentage change
50	0	2	0	2	0	2	0	2	0
50.5	+1%	1.96	-2%	1.953	-2.35%	1.941	-2.95%	1.927	-3.65%
52.5	+5%	1.808	-9.6%	1.774	-11.3%	1.708	-14.6%	1.648	-17.6%
55	+10%	1.633	-18.35%	1.57	-21.5%	1.445	-27.75%	1.33	-33.5%
49.5	-1%	2.041	+2.05%	2.049	+2.45%	2.064	+3.2%	2.076	+3.8%
47.5	-5%	2.216	+10.8%	2.252	+12.6%	2.327	+16.35%	2.392	+19.6%
45	-10%	2.453	+22.65%	2.527	+26.35%	2.68	+34%	2.817	+40.85%

To summarize, for all transmission line types, thinner than designed copper traces have higher impedance, and vice versa. The impedance sensitivity is almost linear for microstrip lines in the simulated range. This sensitivity increases for stripline and CPW when the copper thickness decreases.

3.4.3 Tapered Copper Side Walls

Similar to the RLGC analysis on tapered copper side walls in Section 3.3.4, the copper trace width and gap at the bottom boundary was fixed at an impedance controlled designed value for the SAP method on all three types of transmission lines, leaving the top boundary dimension as the variable. For the embedded case, the top boundary dimensions were fixed instead. This side wall taper reduces the effective copper trace width, which leads to lower capacitance, lower conductance, higher inductance, and higher resistance, with unaffected conductance for SAP fabricated CPW and microstrip

line as exceptions. Overall, tapered copper traces with fixed dimensions at one boundary result in higher impedances. Up to 3 µm width reduction on the variable boundary for all models were simulated. The side wall taper angle is defined in Figure 3.10.

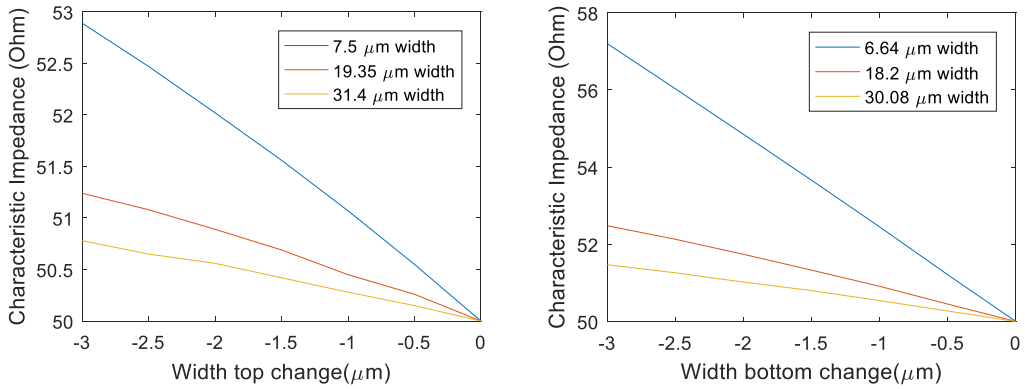


Figure 3.55: Characteristic impedance of 2 µm thick microstrip line with trace top width variation for SAP method (left) and trace bottom width variation for embedded method (right)

For the SAP fabricated microstrip line, the copper trace bottom boundary was fixed, while for the embedded case, the top boundary was fixed. The calculated impedance versus the width change at one boundary is shown in Figure 3.55. According to the simulation results, for the same taper angle, the impedance is more sensitive in narrower microstrip lines. Table 3.18 lists the calculated side wall taper angle for different impedance targets. The typical taper angle for the SAP method in practice is around 85° [33]. For the photo embedded method, this angle is less than or equal to 100° [29], based on the specific material and process parameters used. Therefore, for microstrip lines, this taper effect is insignificant for the SAP method. Even for the

embedded method, the impedance is not sensitive to side wall taper until relatively large angles.

Table 3.18: Calculated microstrip line side wall taper angle for different impedance tolerance

SAP method							
		5 µm ABF, 7.5 µm line bottom width		10 µm ABF, 19.35 µm line bottom width		15 µm ABF, 31.4 µm line bottom width	
Characteristic impedance (Ohm)	Percentage change	Top width (µm)	Side wall taper angle	Top width (µm)	Side wall taper angle	Top width (µm)	Side wall taper angle
50	0	7.5	90º	19.35	90º	31.4	90º
50.5	+1%	7.043	83.5º	18.233	74.4º	29.579	65.5º
52.5	+5%	4.97	57.7º	11.45	26.9º	13.5	12.6º
55	+10%	1.53	33.8º	0.129	11.8º	N/A	N/A
Embedded method							
		5 µm ABF, 6.64 µm line top width		10 µm ABF, 18.2 µm line top width		15 µm ABF, 30.08 µm line top width	
Characteristic impedance (Ohm)	Percentage change	Bottom width (µm)	Side wall taper angle	Bottom width (µm)	Side wall taper angle	Bottom width (µm)	Side wall taper angle
50	0	6.64	90º	18.2	90º	30.08	90º
50.5	+1%	6.435	92.9º	17.65	97.8º	29.15	103.1º
52.5	+5%	5.583	104.8º	15.178	127.1º	24.12	146.1º
55	+10%	4.582	117.2º	10.951	151.1º	12.67	167.1º

For stripline analysis, only the SAP model was selected, due to symmetry as discussed in the previous section. Figure 3.56 shows the calculated impedance versus the top boundary change up to 3 µm. According to the simulation results, for the same taper angle, the impedance is more sensitive to variation for narrower microstrip lines. The side wall taper angle for different impedance targets was calculated for the SAP method, listed in Table 3.18. The taper angle for the embedded method is the supplementary angle of the corresponding SAP case. Similar to the microstrip line, the impedance is more sensitive for narrower striplines, and the typical SAP fabricated side wall angle effect can

be neglected, while the process control is more critical for the embedded method due to its relatively large taper angle.

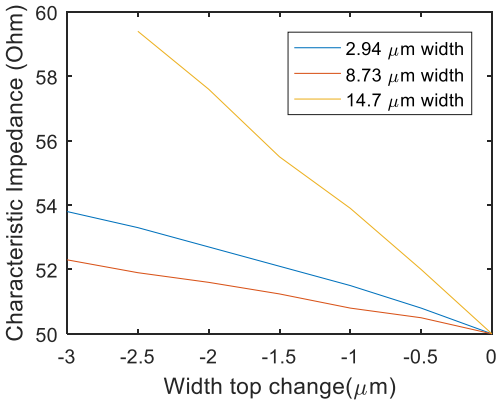


Figure 3.56: Characteristic impedance of 2 µm thick stripline with trace top width variation

Table 3.19: Calculated microstrip line side wall taper angle for different impedance tolerance

		5 µm ABF, 2.94 µm line bottom width		10 µm ABF, 8.73 µm line bottom width		15 µm ABF, 14.7 µm line bottom width	
Characteristic impedance (Ohm)	Percentage change	Top width (µm)	Side wall taper angle	Top width (µm)	Side wall taper angle	Top width (µm)	Side wall taper angle
50	0	2.94	90º	8.73	90º	14.7	90º
50.5	+1%	2.791	87.9º	8.384	85.1º	14.153	82.2º
52.5	+5%	2.26	80.4º	6.87	65.1º	11.33	49.9º
55	+10%	1.5	70.2º	4.458	43.1º	5.932	24.5º

To analyze the side wall taper effect for CPWs, the same assumption was applied as the RLGC analysis in Figure 3.33. The simulated impedance of CPW lines at 5.8 GHz is shown in Figure 3.57. Table 3.20 lists the corresponding side wall angle for 5 µm thick SAP fabricated CPW and 2 µm thick partially embedded CPW at a given impedance tolerance. This taper angle directly affects the effective distance between signal and

ground traces, significantly reducing the capacitive coupling. As a result, the impedance sensitivity to side wall taper angle for CPWs is the most significant among all three types of transmission lines. If the taper angle is difficult to control during fabrication, the compensated design discussed in Section 3.3.4 needs to be used to achieve better impedance control, at the cost of added signal transmission delay.

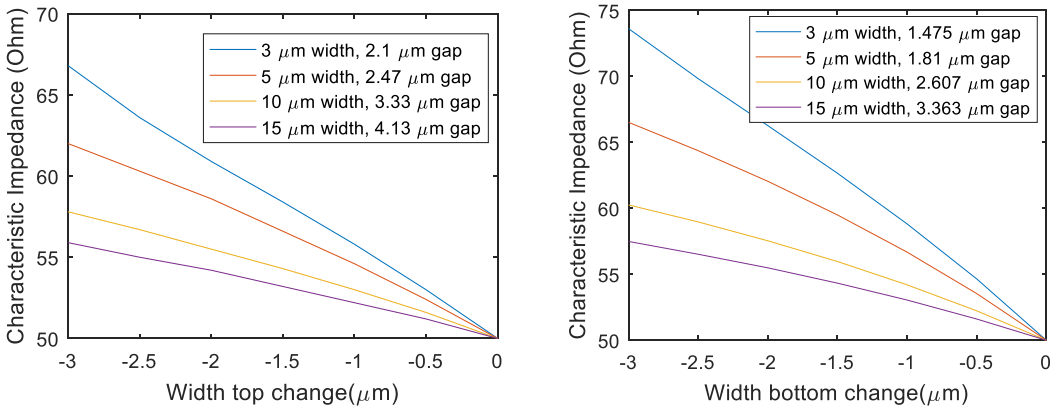


Figure 3.57: Characteristic impedance of CPW versus copper trace top width variation for SAP method (left) and copper trace bottom width variation for embedded method (right)

In summary, for all transmission line types, tapered copper traces lead to higher impedance, and the impedance of CPW is the most sensitive to this effect. A width compensated design can be considered if impedance control is the top priority.

Table 3.20: Calculated microstrip line side wall taper angle for different impedance tolerance

SAP method, 5 µm thick copper, 5 µm ABF									
		3 µm bottom width, 2.1 µm bottom gap		5 µm bottom width, 2.47 µm bottom gap		10 µm bottom width, 3.33 µm bottom gap		15 µm bottom width, 4.13 µm bottom gap	
Characteristic impedance (Ohm)	Percentage change	Top width (µm)	Side wall taper angle	Top width (µm)	Side wall taper angle	Top width (µm)	Side wall taper angle	Top width (µm)	Side wall taper angle
50	0	3	90º	5	90º	10	90º	15	90º
50.5	+1%	2.916	89.5º	4.897	89.4º	9.837	89.1º	14.788	88.8º
52.5	+5%	2.59	87.7º	4.48	87º	9.16	85.2º	13.87	83.6º
55	+10%	2.14	85.1º	3.903	83.7º	8.226	79.9º	12.509	76º
Embedded method, 2 µm thick copper, 5 µm ABF									
		3 µm top width, 1.475 µm top gap		5 µm top width,1.81 µm top gap		10 µm top width, 2.607 µm top gap		15 µm top width, 3.363 µm top gap	
Characteristic impedance (Ohm)	Percentage change	Bottom width (µm)	Side wall taper angle	Bottom width (µm)	Side wall taper angle	Bottom width (µm)	Side wall taper angle	Bottom width (µm)	Side wall taper angle
50	0	3	90º	5	90º	10	90º	15	90º
50.5	+1%	2.95	90.7º	4.934	90.9º	9.895	91.5º	14.851	92.1º
52.5	+5%	2.738	93.7º	4.654	94.9º	9.435	98º	14.179	101.6º
55	+10%	2.46	97.7º	4.274	100.3º	8.778	107º	13.214	114.1º

3.4.4 Copper Surface Roughness

According to the RLGC analysis in Section 3.3.5, only the inductance and capacitance are affected for different surface roughness scenarios. Due to the model solving option being changed from "solve inside" to "solve on boundaries" in order to apply the finite conductivity option to emulate surface roughness, the minor change to the impedance controlled design at 5.8 GHz from Section 3.1 was applied to maintain 50-Ohm impedance in the modified models, as shown in Table 3.21. The characteristic impedance for the same scenarios in Section 3.3.5 of transmission line updated designs were calculated at 5.8 GHz, as shown in Figure 3.58. Even with very rough copper surfaces (1 µm R_a), the impedance increase is roughly 10% for the finest lines. However, if the impedance tolerance is very low for a specific application, and the surface roughness cannot be reduced due to the fabrication process limitations, a compensated design by increasing trace width or thickness is required.

Table 3.21: Updated impedance controlled design for copper surface roughness analysis

SAP method				
Microstrip	Effective dielectric thickness (µm)	Copper thickness (µm)	Signal width (µm)	
	3	2	7.1	
	8	2	18.9	
	13	2	31	
Stripline (Symmetric)	Effective dielectric thickness (µm)	Copper thickness (µm)	Signal width (µm)	
	8	2	2.65	
	18	2	8.39	
	28	2	14.38	
CPW	Effective dielectric thickness (µm)	Copper thickness (µm)	Signal width (µm)	Gap (µm)
	5	5	3	2.26
	5	5	5	2.6
	5	5	10	3.43
	5	5	15	4.22
Embedded method				
Microstrip	Effective dielectric thickness (µm)	Copper thickness (µm)	Signal width (µm)	
	3	2	6.23	
	8	2	17.78	
	13	2	29.66	
CPW	Effective dielectric thickness (µm)	Copper thickness (µm)	Signal width (µm)	Gap (µm)
	3	2	3	1.688
	3	2	5	2.054
	3	2	10	2.866
	3	2	15	3.634

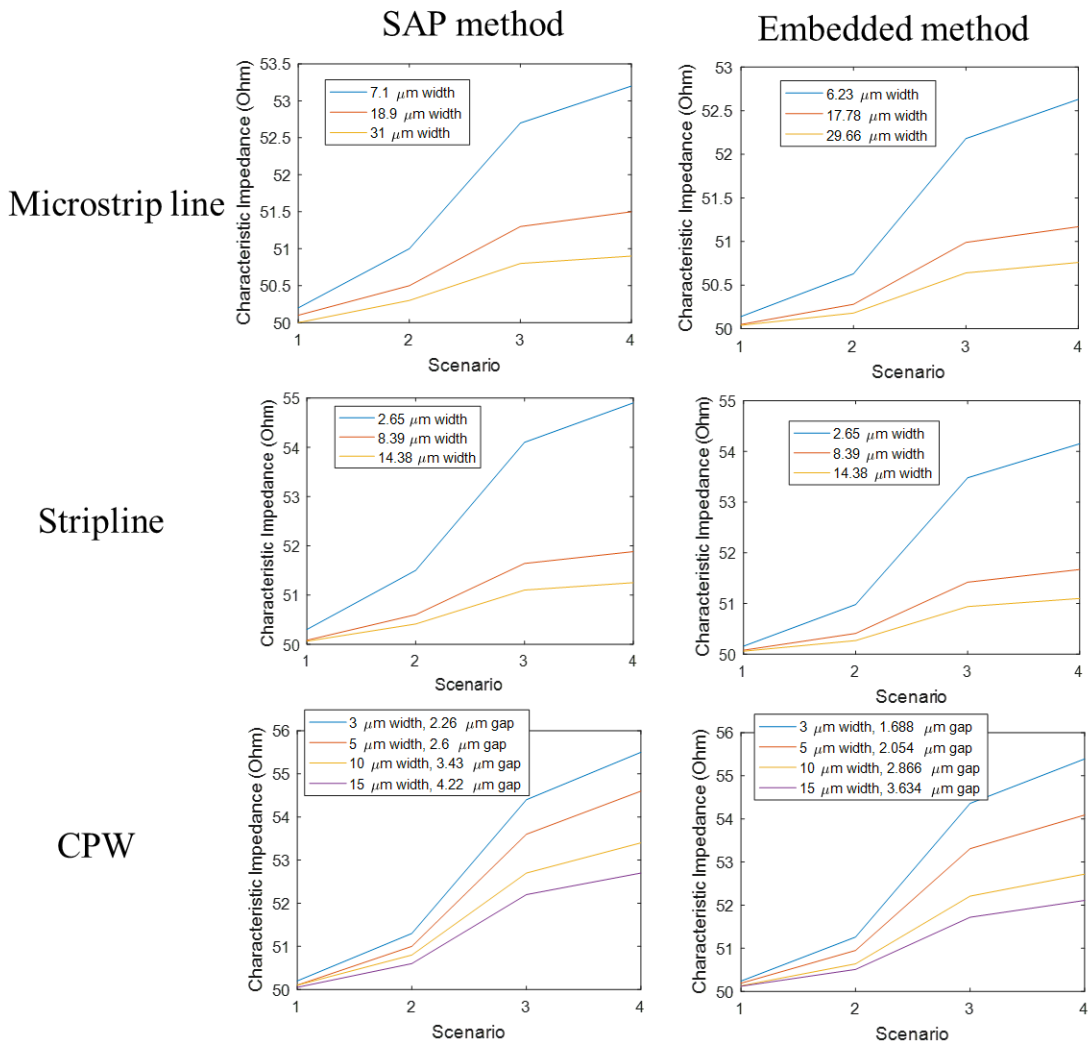


Figure 3.58: Impedance of transmission lines with different copper surface roughness scenarios

In addition to the impedance analysis, a 3D HFSS model was established for 1 mm long transmission lines of all types with the surface roughness boundary conditions. The solution type was set to “DrivenTerminal” for wave ports, with maximum delta S set to 0.5%. The surface roughness model for HFSS is a Groisse model, which is different

from the one used in 2D extractor models. In the Groisse model, the conductivity of the conductor is modified by

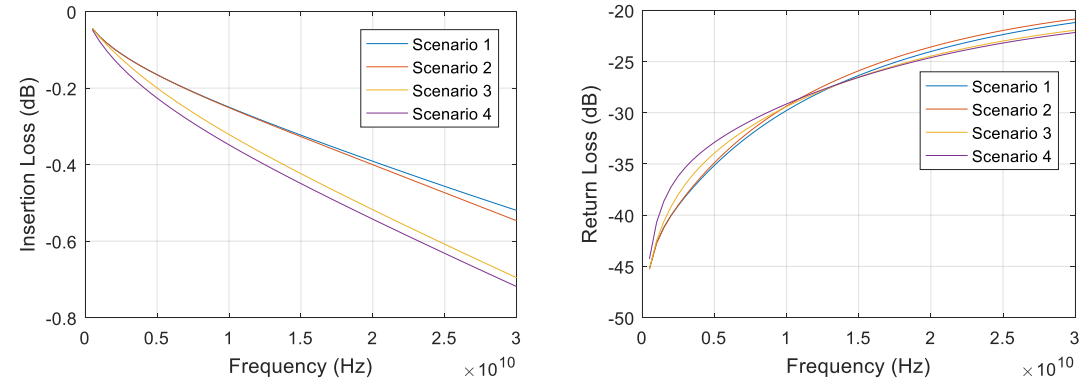
$$\sigma_c = \frac{\sigma}{K_w^{\ 2}} \tag{3.9}$$

where σ is the material's conductivity. The Groisse coefficient K_w is given by

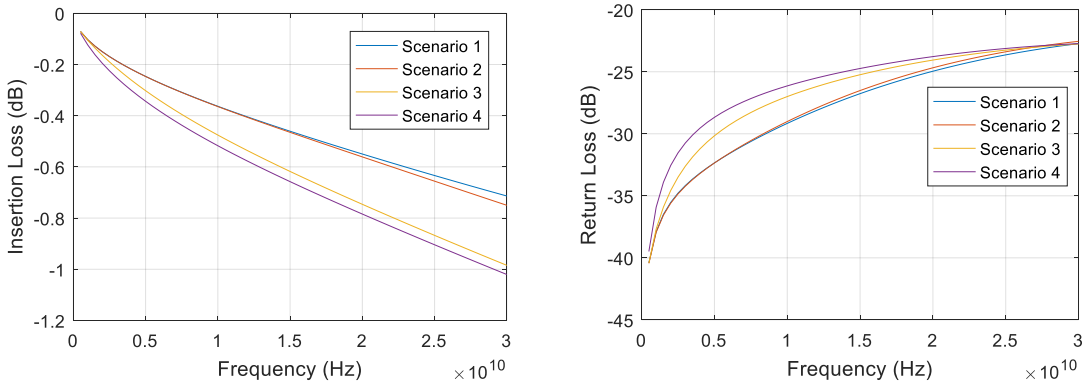
$$K_w = 1 + \exp\left(-\left(\frac{\delta_s}{2R_a} \right)^{1.6} \right) \tag{3.10}$$

where δ_s is the skin depth and R_a is the RMS surface roughness value.

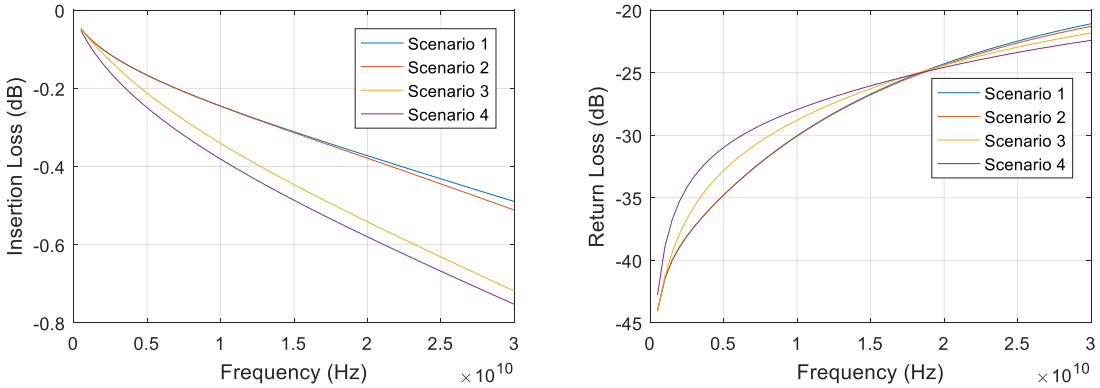
For SAP fabricated transmission lines, the simulated insertion loss and return loss are shown in Figure 3.59. The transmission lines produced by the embedded method were simulated as well, with the S-parameters shown in Figure 3.60. Only the first row of each transmission line type in Table 3.21 were selected to study the surface roughness impact on S-parameters. According to the simulation results, the insertion loss increases dramatically starting from Scenario 3 for both fabrication methods due to higher conductor loss, while the return loss is mainly affected by impedance mismatch.



(a)

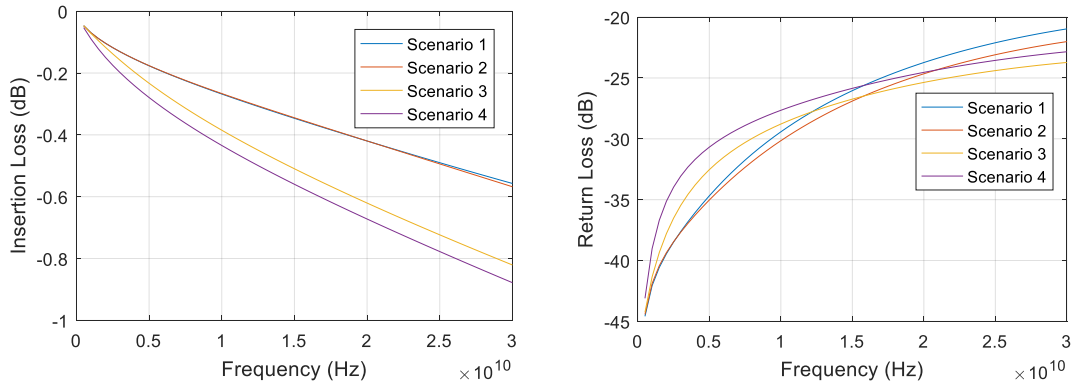


(b)

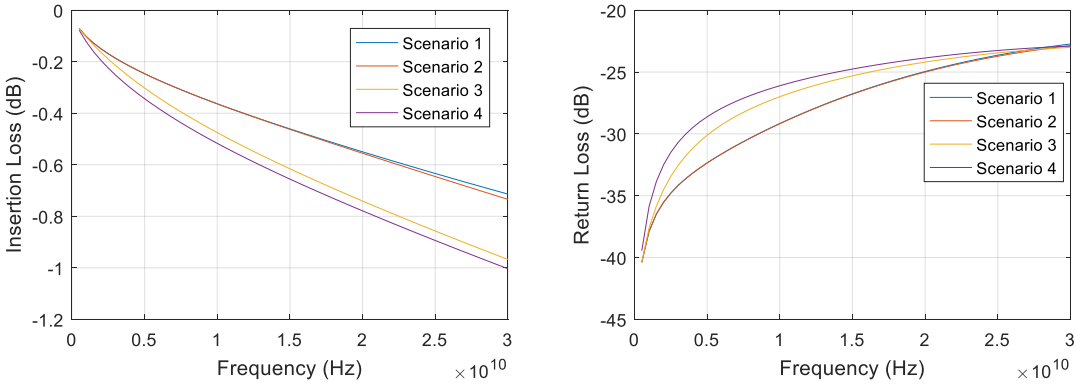


(c)

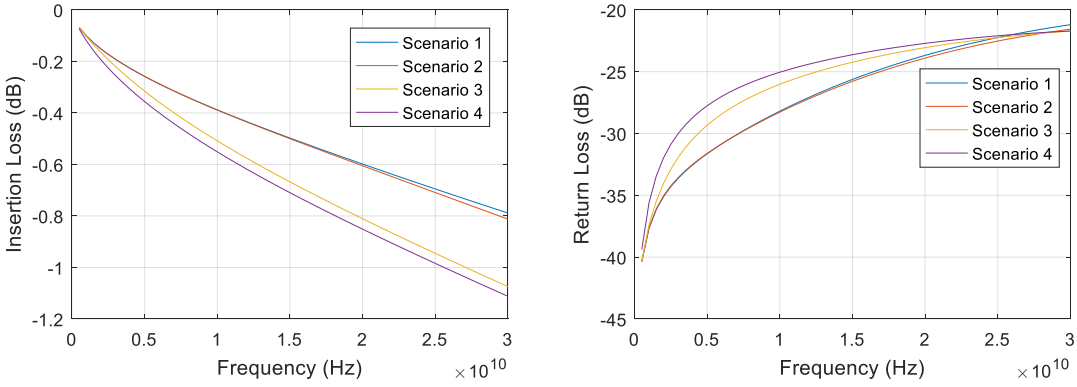
Figure 3.59: Simulated insertion loss and return loss of 1 mm long (a) microstrip line, (b) stripline, and (c) CPW with different surface roughness scenarios, fabricated by SAP method



(a)



(b)



(c)

Figure 3.60: Simulated insertion loss and return loss of 1 mm long (a) microstrip line, (b) stripline, and (c) CPW with different surface roughness scenarios, fabricated by embedded method

To summarize, the copper surface roughness added to the 2D model increases the characteristic impedance across all types of transmission lines. The impedance is not affected significantly compared to all other process variations. The major impact of surface roughness is conductor loss due to lower conductivity on rough copper surfaces.

3.5 Chapter Summary

1. Impedance controlled transmission line design rule for interposer RDL: The current SAP method and the emerging embedded method were considered for creating a set of process design rules. Epoxy based ABF GX 92 polymer dielectric with 5 μm, 10 μm, and 15 μm thickness was selected for microstrip line, stripline, and CPW design with 50 Ohm impedance control at 5.8 GHz. In addition, microstrip line and stripline design rules with 2 μm width and 3 μm copper thickness were provided with the required material thickness to provide a roadmap for future material development.

2. SAP and Embedded Process Variations: Both the SAP method and embedded methods introduce process variations, resulting in non-ideal shaped lines. The process steps of copper seed layer deposition, photolithography, copper electrolytic plating, seed layer etching, and polymer trench formation were discussed to identity the sources of variations and their impact on the line shape.

3. Impact of Process Variations on Electrical Performance: Four critical process variations for the SAP and embedded methods were chosen to study their impact on electrical performance. These are: (1) copper trace width, (2) copper thickness, (3) side wall taper, and (4) copper surface roughness. For all transmission line types, reducing

copper trace width or thickness leads to lower capacitance, lower conductance, higher inductance, and higher resistance. For copper side wall taper angle analysis, if the trace wider boundary width is equal to the impedance controlled design value, then tapered copper traces always lead to lower capacitance, lower conductance, higher inductance, and higher resistance, with unaffected conductance for SAP fabricated CPW and microstrip line as exceptions. The taper effect can be compensated by increasing the copper width, and the impedance controlled design for copper traces with tapered side walls were calculated. Even with good impedance control, the non-vertical side wall increases RLGC parasitic elements and degrades signal integrity, with exceptions of microstrip lines formed by the embedded method. The tapered copper trace with impedance controlled design for a partially embedded microstrip line showed marginally better electrical performance (0.04 dB/mm less insertion loss at 30 GHz for around 7-8 μm width microstrip line) at the cost of wiring density. Copper surface roughness only affects the inductance and capacitance for all types of transmission lines.

4. Impedance Sensitivity to Process Variations: The impedance sensitivity of four process variations were analyzed. For all transmission line types, narrower than designed signal trace width results in higher impedance, and vice versa. The impedance sensitivity to width increases when the width reduces for microstrip line and stripline. The width tolerance for an SAP fabricated microstrip line with 7.5 μm designed width is -8.27% to +9.2% for 5% impedance tolerance. Such width tolerance is slightly larger for a partially embedded microstrip line, which is -9.4% to +9.35% for 6.64 μm original width. For 2.94 μm stripline, the 5% impedance target yields the width tolerance of -11.8% to +13.1%. The impedance is more sensitive for CPWs with a narrower gap, with -6% to +5.67%

width tolerance for a 3 μm width, 2.1 μm gap and 5 μm thick CPW produced by the SAP method to achieve 5% impedance tolerance target. The partially embedded CPW with thinner copper thickness (2 μm) and narrow gap (1.475 μm) but same width (3 μm) has a more strict width tolerance (-4.57% to +4.53%) to achieve the same 5% impedance tolerance target. Reducing the copper thickness increases the impedance of all three types of transmission lines. The impedance sensitivity is almost linear for microstrip lines within the simulated range of process variations. Specifically, -12% to +12% thickness tolerance on 2 μm thick, 7.5 μm wide SAP fabricated microstrip line to control the impedance within 5% error. This range is -11.3% to +11.25% for the embedded case. However, this sensitivity increases for stripline and CPW when the copper thickness decreases. For stripline's case, an impedance error below 5% requires the thickness to be controlled within -9% to +11.5% for 2.94 μm width and 2 μm thick line. Tapered copper traces result in higher impedances when the maximum width of the transmission lines are fixed at the designed parameter. The CPW is the most impedance sensitive transmission line type to this effect. The side wall angle for a SAP fabricated CPW needs to be higher than 87.7° to keep the impedance lower than 52.5 Ohm, which is a 5% increase. For a SAP fabricated microstrip line and strip line, this side wall angle is 57.7° and 80.4°. Width compensated designs can be considered if impedance control is the top priority. Copper surface roughness has the least significant impact on the impedance among all four process variations analyzed. The 0.1 μm copper surface roughness increases the impedance of all types of transmission lines by less than 3%, and 1 μm extreme rough copper increases the impedance up to 11%. However, the conductor loss is directly affected by increased conductor surface roughness. The 1 μm extreme rough copper can

increase the insertion loss by up to 0.3 dB/mm at 30 GHz for a partially embedded microstrip line. If the insertion loss is of major concern for the specified application, the copper surface needs to be fabricated as smooth as possible.

CHAPTER 4

PANEL SCALE SEMI-ADDITIVE PROCESS (SAP) ADVANCES TO ACHIEVE CONTROLLED IMPEDANCE FOR 2 MICRON LINE WIDTHS

In the previous chapter, the impact of process variations on the electrical performance was analyzed for three common types of package transmission lines, and the process tolerances required to meet different impedance tolerance targets were provided, leading to preliminary design guidelines for process control. This chapter discusses the process advances in critical process steps in the SAP method on glass interposers to achieve 2 μm width transmission lines, but with improved line width and shape control. In contrast to prior work using liquid photoresists and silicon wafer processes, this dissertation demonstrates ultra-fine lines using dry film photoresists and panel processes on thin glass substrates. The standard SAP process flow schematic is shown in Figure 4.1. The thin glass was covered by polymer dielectric layers on both sides, followed by copper seed layer deposition. The lithography process on the copper seed layer was improved to achieve 2 μm resolution, as it is one of the key aspects that limits the minimum feature size and process tolerance of the SAP method. A novel ozone treatment was proposed and demonstrated as a higher throughput alternative to traditional plasma treatment for surface modification and cleaning to improve RDL process control and yield. Several copper seed layer etch technologies were tested and compared for best line shape control. Finally, a cost-effective surface planarization process was proposed and

optimized to improve copper thickness uniformity and thin down the dielectric polymer to achieve the target 50-ohm impedance with a high degree of control.

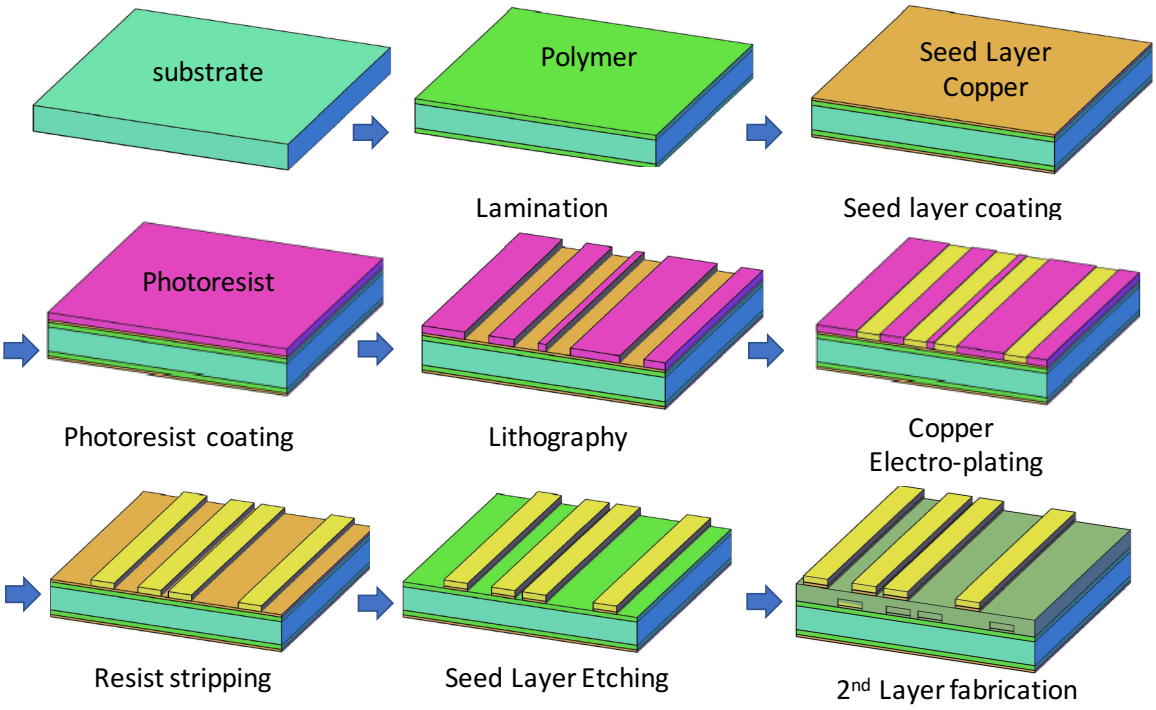


Figure 4.1: Standard Semi-Additive Process Flow

4.1 Glass Substrate Preparation, Dry Film Polymer Lamination and Copper Seed Layer Deposition

Panel-based glass interposers have been demonstrated as a lower cost and higher performance alternative, to address the I/O density challenges of organic packages, and the cost and performance challenges of silicon interposers [12-15]. Thin polymer dielectric layers are used to fabricate RDL wiring on the surface of the glass, and such a polymer layer also assists in the handling of the thin glass panels, due to its low elastic modulus. Epoxy dry films (ABF from Ajinomoto, Japan) were chosen for this research

due to their ease of panel processing, high flow for planarity over underlying circuits, and compatibility with electroless copper seed layer plating. This new generation of polymer dielectric has a smooth surface, which enables higher photolithographic resolution than conventional polymers with high degree of surface roughness. Before polymer lamination, a silane surface treatment process was applied to the glass panel to increase adhesion between the polymer and glass, preventing delamination during subsequent processing and enhancing the interposer reliability. The polymer lamination was conducted in a vacuum laminator, followed by a hot-press process to enhance the polymer surface planarity. The polymer was then thermally cured in an oven for one hour at 180˚C. The copper seed layer on the polymer for SAP was formed by electroless plating, which is a high throughput, and low temperature wet process compared to physical vapor deposition (PVD), and scalable to large panels and double side processing. Figure 4.2 shows the 6-inch polymer laminated glass panel after electroless copper seed layer deposition. The seed layer does not extend all the way to the edge of the panel due to the edge framing used to support the panel in the plating baths.

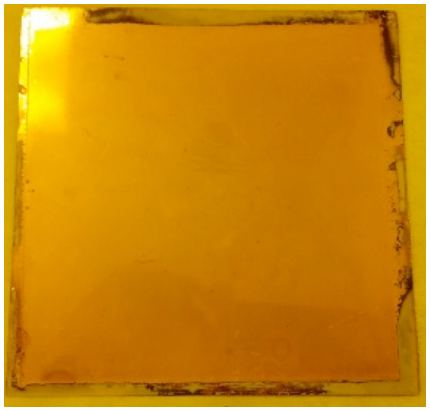


Figure 4.2: Six-inch polymer laminated glass panel with electroless copper seed layer

4.2 Lithography Process & Line Width Control for 2 µm CDs

Photolithography is the most commonly used process method to fabricate ultra-small features such as transistors and fine line wiring on transistor wafers and on interposers and package substrates. Most of the current package substrate processes utilize i-line UV lithography at 365nm wavelength, in large field size exposure mode or in stepper mode for higher resolution but lower throughput. The resolution of the lithography process is one of the key aspects that limits the minimum feature size of the SAP method. This resolution is limited by two types of factors, (a) material and process factors such as the photoresist material, the adhesion strength of the photoresist to the substrate, and the lithography tools, and (b) substrate factors such as the planarity and roughness of the substrate core. A rough and non-planar surface will negatively impact the lithographic resolution. Organic substrates have larger thickness variation and a rougher surface compared to glass substrates, due to the glass fabric woven inside the organic core. Therefore, lithography on glass is expected to have better yields than on organic substrates at 2-5 µm feature sizes for the same lithography process conditions.

Two forms of photoresist are commonly used for lithography, namely, liquid photoresists, and dry film resists (DFR). In general, DFRs have lower cost and are better suited for double side processing on large panels than liquid photoresists. High resolution DFRs with thickness of 7 µm, 10 µm, and 15 µm provided by Hitachi Chemical [37] were used in this study. To enhance the adhesion between DFR and the copper seed layer surface, an adhesion promoter treatment under development by Atotech was applied. This surface treatment process called Novalink^{TM} has been proven to significantly increase the

lithography process yield at 5 μm feature size, and enables higher lithographic resolution below 5 μm.

A glass photomask consisting of comb structures, escape routing structures, and CPW lines was used for the lithography process. The lithography process flow is summarized in Figure 4.3. The adhesion promoter treatment has two steps, called Novalink ME and Novalink MES. After the treatment, the copper seed layer surface turned matte, as shown in Figure 4.4. Fine line patterns with feature sizes of 2-5 μm were achieved with the appropriate lithography tool, high resolution DFR, and adhesion promoter treatment, as described below.

Ushio's new advanced projection lithography tool Ushio UX-44101 [38] was set up at the Georgia Tech PRC. This machine is a specialized projection lithography tool for panel-based fabrication, and has a 2 μm resolution and 70 mm x 70 mm large exposure area. This large exposure area enables high throughput step-and-repeat exposure, suitable for high-volume manufacturing of full-panel size interposers in the near future. Another unique feature of this tool is the +/- 10 μm depth of focus, essential to accommodate non-planarity, and warpage of the panels and variation of work thickness. Table 4.1 summarizes the key specifications of this lithography tool. This lithography tool, along with high resolution DFR and proper surface treatment, can support the patterned feature size down to 2 μm. The DFR applied in this experiment was 7 μm thick, a complete design of experiments (DoE) was conducted to arrive at an optimum exposure dose of 180 mJ/cm^2. The development was done in a spray developing tool with spray nozzles located on both sides of a horizontal conveyer on which the panels were placed. The development chemistry used was 1 volume % sodium carbonate, and the conveyer

speed for the DFR development was set to 40 inch/min. The SEM image of the developed DFR structures with 2 μm line and space pattern is shown in Figure 4.5. This figure also shows the limitation of this lithography process, as the 1.5 μm trench structure did not yield and the DFR structure collapsed. For 7 μm thick DFR, the aspect ratio of 1.5 μm line and space pattern is 4.67, and the stiffness of this DFR is not high enough to support such a high aspect ratio structure. To further improve the lithographic resolution, the thickness of the DFR needs to be reduced or the stiffness needs to be increased.

Table 4.1: UX-44101 projection lithography tool specifications

Resolution	< 2 μm L/S
Effective exposure field	70 mm x 70 mm
Wavelength	365 nm (i-line)
Depth of Focus (DOF)	+/- 10 μm
Alignment accuracy	<1 μm

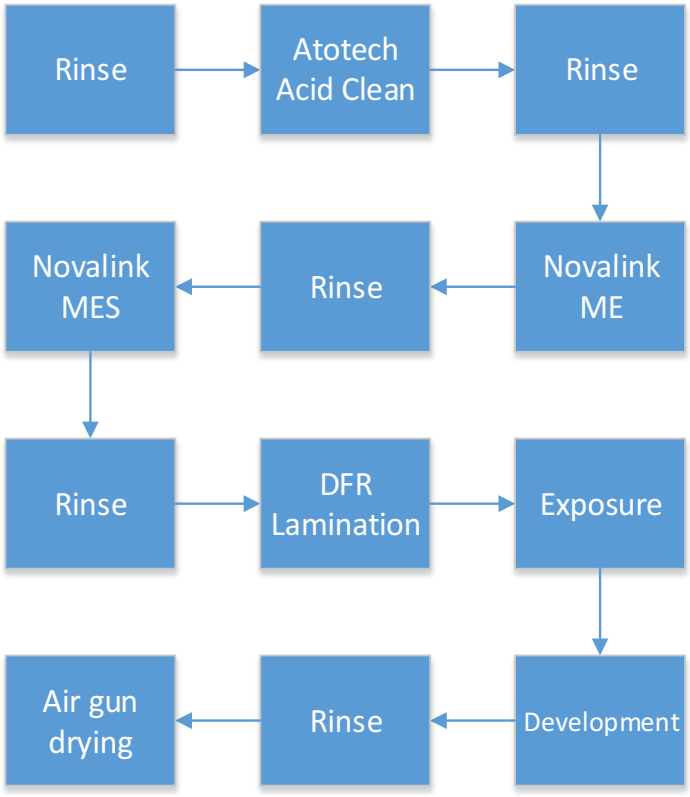


Figure 4.3: High resolution lithography process flow chart

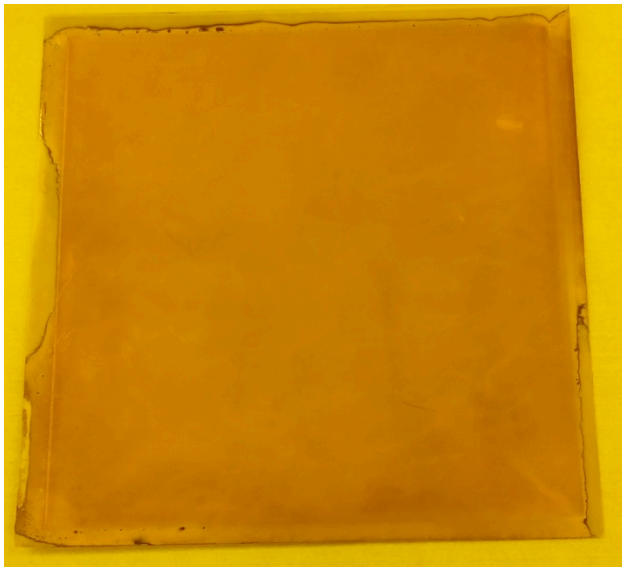


Figure 4.4: Copper seed layer on polymer laminated glass panel after Novalink treatment

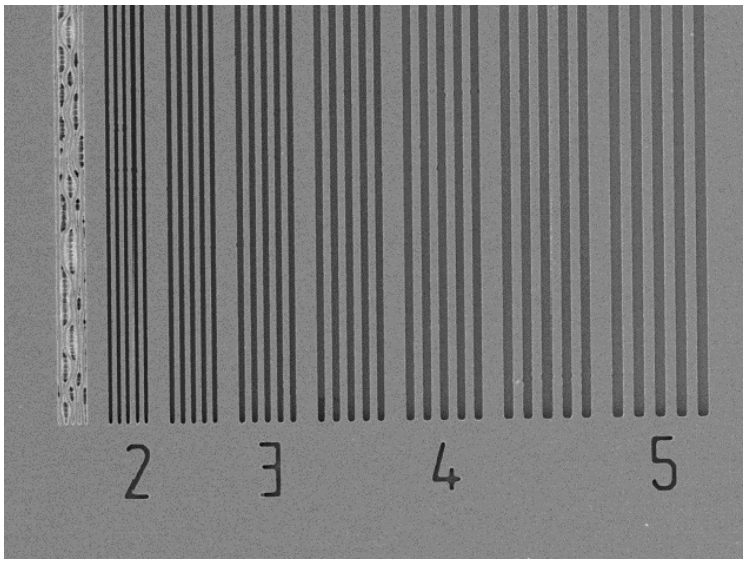


Figure 4.5: SEM image of patterned DFR trenches from 2 µm line and space to 5 µm line and space

4.3 Copper Metallization and Ozone Treatment to Improve RDL Yield and Improve Line Shape

The copper RDL structures on glass interposers were metallized by electrolytic plating. The plating chemistry was from Atotech, called Cupracid TP [39]. It contains "Electropure Copper Sulfate sol.", sulfuric acid, sodium chloride, along with organic additives including "Cupracid TP Leveller", "Cupracid Brightener", and is mixed with a "Cupracid Starter" solution. To maintain good copper thickness uniformity and a smooth plated surface for better signal integrity, the ratio of inorganic and organic additives in the plating tank needs to be controlled at an optimal value recommended by the chemistry provider. The copper layer thickness was determined by the electrolytic plating time and current density, which can be calculated theoretically using equation (3.4) in the previous

chapter. A stripping solvent was used to remove the DFR following the electrolytic copper plating process.

Typically, a 5-minute plasma etching by O_2 gas is used after the develop step and before the plating step, removing any DFR residue in the trench and improving the wettability of the copper surface for better plating quality. A novel high throughput and atmospheric ozone treatment process was demonstrated in this research instead of the standard plasma etching process before copper electrolytic plating, as well as for cleaning the DFR residue on the copper seed layer after DFR stripping step in the solvent. These two key steps are essential to maintain the copper trace quality and yield. For the first time, this innovative approach was tested to demonstrate the effectiveness for wettability improvement and DFR residue cleaning. Ozone treatment offers a practical and environmentally friendly alternative to both traditional chemical wet cleans, which incur water treatment costs to dispose of hazardous chemicals, and oxygen plasma processes, which require a vacuum chamber. The ozone process scales easily, allowing for application to both wafers and large panels. Ozone treatment improves copper plating quality by enhancing the surface energy on DFR and copper seed layer, increasing the wettability of copper and DFR mixed surface, as well as removing the organic contaminants that negatively affect the wettability and plating yield. The target of this study was to illustrate the effectiveness and benefits of the processes developed using an MKS ozone delivery system. The figures of merit for these ozone processes are discussed in the following paragraph, namely the improvement in residual DFR removal and the use of contact angle measurement to quantify the hydrophilicity of plating surfaces.

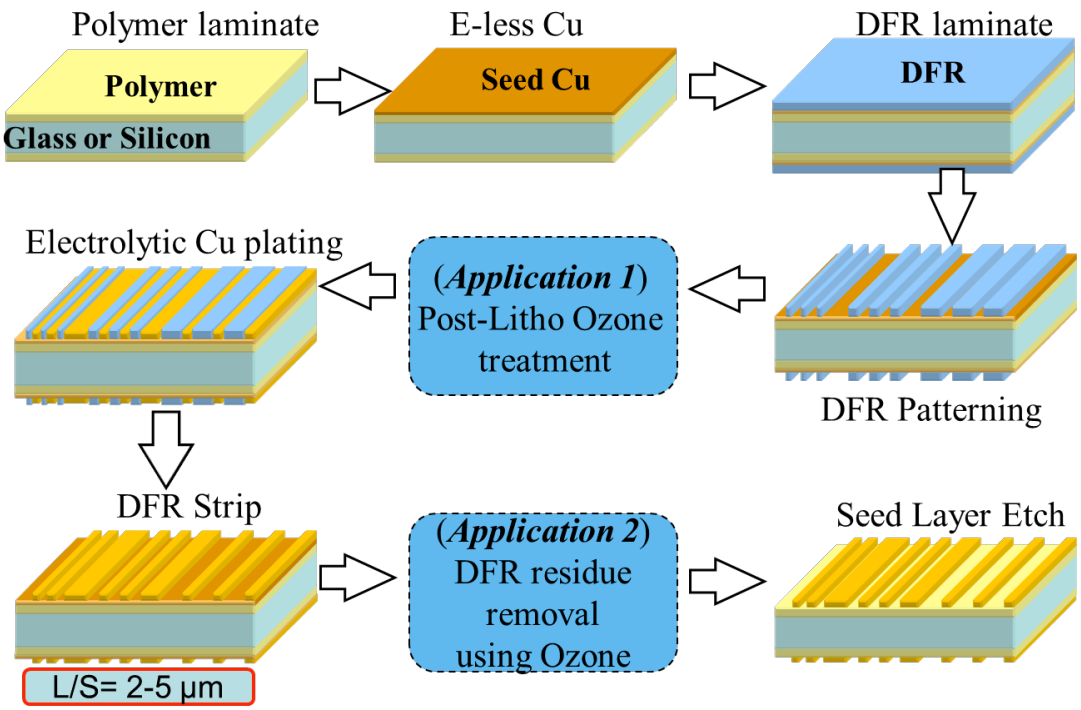


Figure 4.6: Two potential applications of ozone treatments evaluated in a SAP flow for RDL fabrication

Figure 4.6 shows the ozone process step integrated into the SAP flow for quality and yield improvements in fine-line RDL fabrication. The glass substrate preparation step and photo lithography process were unaltered. After lithography, a plasma treatment process is commonly used to clean up any resist residue from the plating surfaces as well as to improve the wettability of this surface for high plating yields. This is the first potential application for ozone treatment as an alternative to plasma treatments. After the treatment (plasma or ozone) the RDL structures were built up by electroplating copper on the seed layer exposed during the lithography step. The second potential application for ozone treatment is between the DFR strip and the copper seed layer etch. Any DFR

residue after strip prior to seed layer etch causes incomplete removal of the seed layer, resulting in electrical shorts between the RDL lines which reduces panel yields.

MKS provided a standalone two channel ozone delivery system (AX8550-247ECB6-42C) with two integrated ozone generators, an ozone concentration monitor and pressure control system that enables desired output of ozone from the generators from 6 SLM to 20 SLM O_2 flow with ozone concentration tunable up to 350 g/Nm^3 [40], installed in the PRC, as shown in Figure 4.7. For the following experiments, the substrates were treated with ozone at a concentration of 300g/Nm^3. The ozone gas is delivered at atmospheric pressure to a box chamber with a hot plate installed wherein the panels were placed. The unused gas is then passed through a catalytic ozone destruction system that converts any unused O_3 back to O_2 before releasing to process exhaust. Since there is no electrical/RF bias required on the substrate platen as is the case for plasma treatment systems, as well as no vacuum pump requirements, the process chambers can be very cost effective and easily scalable for high volume manufacturing using double side compatible processes. Furthermore, there are no concerns for uniformity of the treatment (as is often the case in plasma treatment systems) as long as sufficient ozone is supplied to the process chamber. Lastly, a single ozone delivery system can be configured to support multiple process chambers via the multichannel output configuration available on MKS's ozone delivery systems.

Figure 4.7: Setup of the ozone treatment system at PRC. The ozone delivery system is on the right while the "box" chamber is shown on the left. The exhaust from the chamber is routed to an ozone destruct (not shown) to convert any unused ozone to oxygen.

RDL test patterns fabricated using ozone and oxygen plasma treatment were compared with a control sample with no treatment, to study the suitability of the ozone treatment for wafer-scale and panel-scale processing. All samples received identical lamination, copper seed layer deposition, and lithography steps. Surface treatment by either oxygen plasma or ozone was then introduced for some samples prior to electroplating. Figure 4.8 and Figure 4.9 illustrate the differences in RDL line features post-plating.

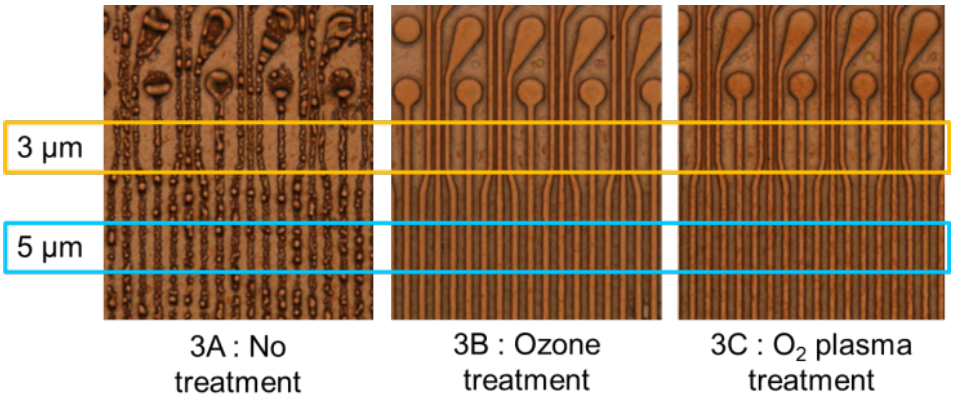


Figure 4.8: Comparison of fine line RDL features after copper electroplating on substrates with no treatment (3A), ozone treatment (3B), and O2 plasma treatments (3C) illustrating the improvement in plated line quality resulting from wettability improvements of the surfaces with plasma or Ozone treatments

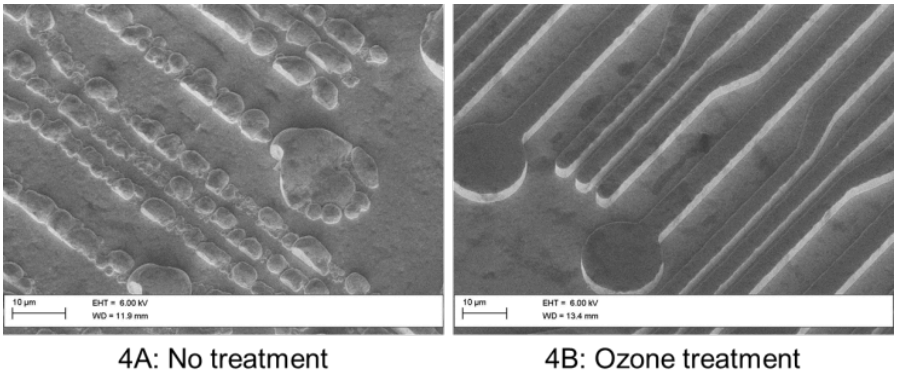


Figure 4.9: SEM image comparison of fine line RDL after copper electroplating on substrates with no treatment (4A) and ozone treatment (4B)

The RDL features on the untreated surface were poorly defined whereas the RDL features were well defined at both the 3 µm and 5 µm feature sizes after the copper seed layer surfaces were treated with either ozone or oxygen plasma. The issue with an untreated sample is that organic residue on the copper seed layer exposed after lithography negatively impacts the hydrophilicity of the substrate surface. Without proper

surface modification, there is insufficient wetting of surfaces in the electroplating bath, which results in non-uniform plating and high resistance RDL structures. Thus, a surface treatment step using an oxygen plasma or ozone treatment prior to the plating step significantly improves the plating process yields by effectively removing any organic residues from the seed layer surface and resulting in well-defined traces. One significant benefit of the ozone or oxygen plasma treatments prior to plating is the significant improvement in the wettability of all the surface regions on the panel to be plated as measured through water contact angle measurements (Figure 4.10). Both the ozone and oxygen plasma treated samples show significantly lower water contact angles on substrates prepared using two different seed layer deposition methods, (A) PVD Cu and (B) Electroless Cu deposition. It is notable that the wettability improvement was observed on all regions of the substrate. The copper seed layer, the DFR covered regions and the DFR mesh patterned surfaces indicated a uniform increase in the hydrophilicity of the surface that can help with uniform plating across the entire panel surface. This result implies that plating yields on large area substrates and panels would benefit from the addition of an ozone treatment step prior to electroplating. In addition, the ozone treated sample had slightly wider metallized copper traces than the oxygen plasma treated samples under the same photo-lithographic conditions. This is due to the higher amount of DFR etch during the ozone treatment compared to the plasma treatment. Figure 4.11 shows the DFR trench etched by ozone after the treatment. The trench width increased to 7 μm from 5.7 μm, resulting in wider copper traces after plating. This 1.3 μm width increase is within 10% impedance tolerance for microstrip lines of 7.5 μm and larger, but exceeds 10% impedance tolerance for 2.94 μm stripline. For the design compensation,

this DFR etching effect needs to be considered. For comparison, the traditional oxygen plasma treatment increases the DFR trench width by mere 0.3 µm, where less design compensation is required.

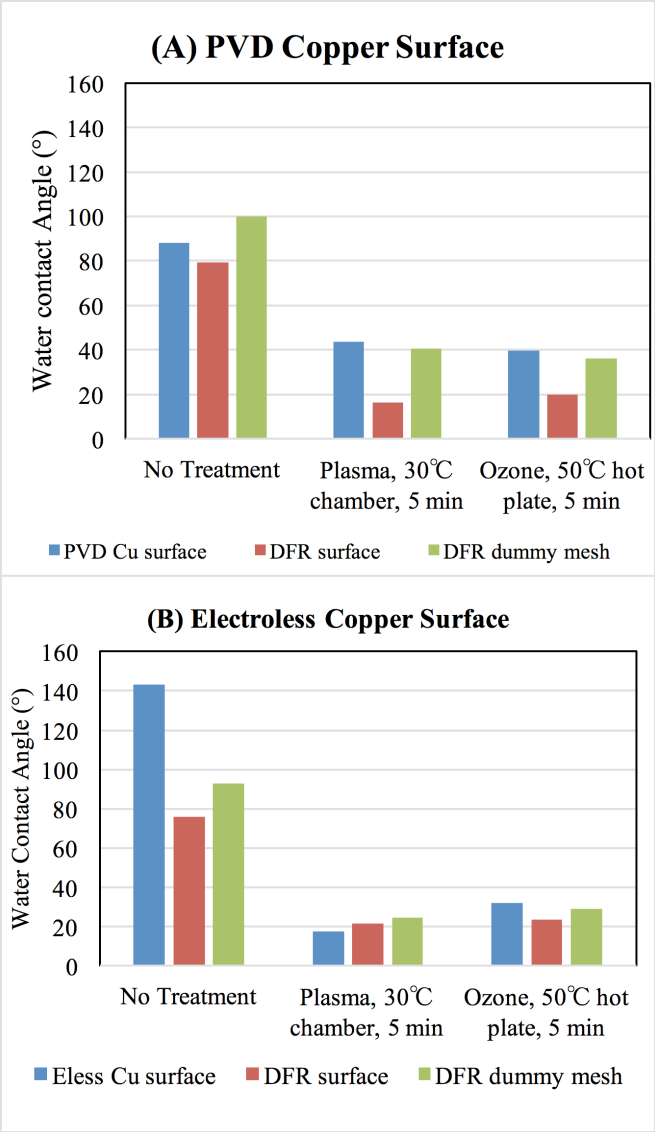


Figure 4.10: Comparison of water contact angle (wettability) of the various regions on the panel surface on substrates with No treatment, O2 plasma treatment or ozone treatments on two types of Cu Seed layers deposited using PVD (A) or electroless Cu (B)

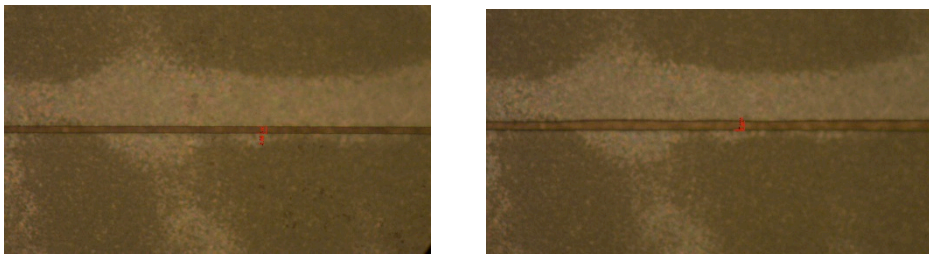


Figure 4.11: DFR trench before (left) and after (right) ozone treatment. The measured gap width was 5.7 µm before ozone treatment and 7 µm after ozone treatment on the same location

The improvements in RDL fabrication resulting from ozone or oxygen plasma treatments were further quantified through yield measurements of 2 mm long copper lines with widths of 8 µm or 5 µm. Four-point resistance measurements of the lines were made as illustrated in Figure 4.12. The lines were considered acceptable if the line resistance was measured to be lower than a specified threshold since lines with multiple defects had significantly higher line resistance. Multiple defects in the lines of the samples with no treatment resulted in extremely high trace resistance and 0% yield. In contrast, samples prepared using the same process but having an additional ozone treatment had visually no defects and 100% yields as quantified in Table 4.2. Similar improvements were also observed on samples with oxygen plasma treatment. These improvements, though illustrative of a lab process, underscore the need for surface preparation and cleanliness as a necessary step in the integration flow for high volume industrial implementation of the SAP RDL as the CDs scale to 2 µm.

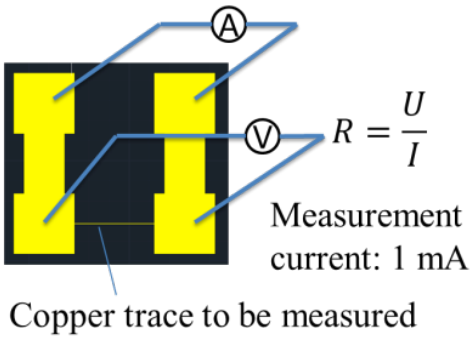


Figure 4.12: Structure used for measuring line resistance and RDL yield. Copper trace has 2 mm in length, 5 µm or 8 µm in width.

Table 4.2: RDL trace line yields measured for samples processed with no treatment and with ozone treatment prior to plating step

Trace No.	Width	Length	No Treatment	Ozone Treatment
1	8 µm	2 mm	0 %	100%
2	5 µm	2 mm	0 %	100%

The second potential ozone application in the manufacturing flow is in the removal of any DFR residue after the resist strip step. Residual DFR negatively affects the subsequent removal of the copper seed layer, especially in processes where RDL fabrication requires thicker DFR films to achieve higher aspect ratios for lower trace resistance. A closer inspection of a typical DFR residue defect is shown in Figure 4.13, where the same region of the sample was observed at different stages in the process flow. Both sample 1 and sample 2 show DFR residues after the DFR strip. Sample 1, directly taken to the seed layer etch steps, retained the DFR residue on the surface resulting in partial removal of the seed layer. Sample 2 that went through an ozone treatment (150 °C,

5 min) shows complete removal of DFR residue from the surface and resulted in complete removal of the seed layer thus yielding a defect free panel.

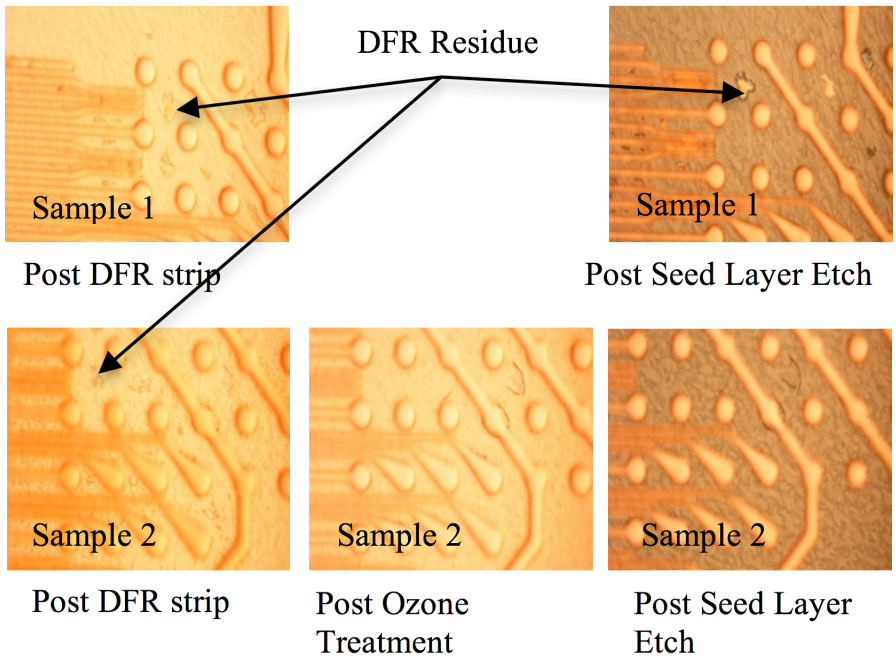


Figure 4.13: Removal of DFR residue after strip using ozone treatment on Sample 2, compared to Sample 1 without ozone treatment

4.4 Copper Seed Layer Etching and Line Width Variation Control

The copper seed layer etching was the last step to obtain the designed one metal layer RDL patterns. This critical process determines the limitation of the SAP method for fine line RDL scaling as well as line width tolerance, since it is the only step in the SAP process flow that involves wet etching of copper. The standard immersion wet etching process is isotropic, which is not ideal for fine line SAP, as depicted in Figure 4.14. For a single line structure, the copper trace side wall and top is etched at the same rate as the seed layer, resulting in narrower and lower line profiles as well as undercut. For line and space patterns below 8 μm, the ability of the etching solution to penetrate the narrow and

high aspect ratio trenches between copper traces becomes a further challenge. As a result, the etching speed of the copper traces is faster than the seed layer, causing over etch and undercut of copper traces. This leads to trapezoidal shaped lines, rough copper surfaces, and even delamination of ultra-fine copper traces. Therefore, this etching method is suitable for large copper patterns but not for fine line RDL fabrication.

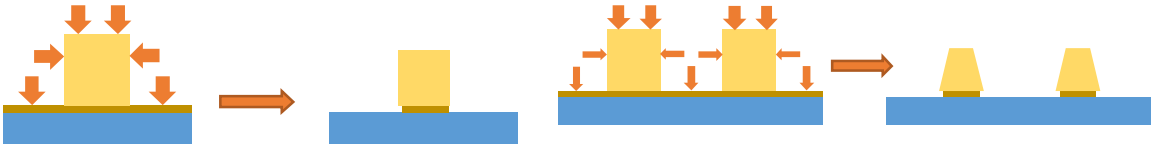


Figure 4.14: Standard immersion seed layer wet etching on single trace (left) and high-density routing (right). Etching speed independent of direction and copper type

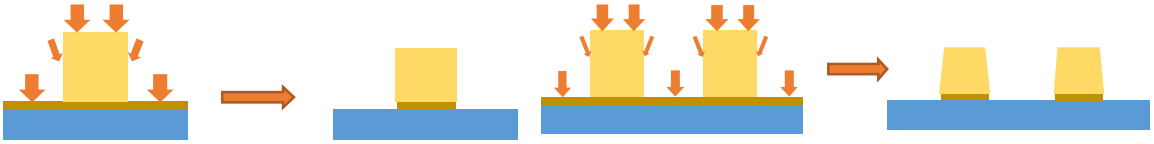


Figure 4.15: Standard spray seed layer wet etching on single trace (left) and high-density routing (right). Etching speed dependent of direction

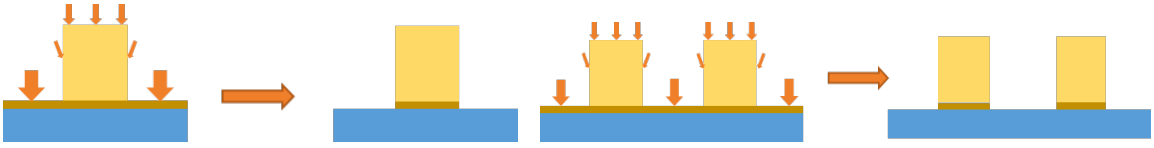


Figure 4.16: Spray etching with differential etchant on single trace (left) and high-density routing (right). Etching speed dependent of direction and copper type

A seed layer etching process with adequate selectivity is required to fabricate 2 µm features and enable the line densities required for 2.5D integration. A spray etching

method increases the selectivity of the etching direction, causing higher vertical etching speed than lateral etching speed (Figure 4.15). Similar to the immersion seed layer etching process, the copper surface is attacked by the etchant, resulting in a rough copper surface. To further improve the anisotropy of the seed layer etching process, differential etchant chemistries have been developed by Atotech called CupraEtch DE [41]. Such chemistries have special additives that passivate the electroplated copper sidewall during etching, and also create a differential etch rate with the copper seed layer etching at twice the rate of the electrolytic plated copper, driven by the different grain structures. This etchant also yields smoother copper surfaces after seed layer removal. By combining the spray etching method with the differential etchant, a novel high selectivity etching approach was developed for fine line RDL fabrication as shown in Figure 4.16.

Figure 4.17: The cross-sectional image of 5 µm line and space pattern after immerge seed layer etching (left) and differential etching (right)

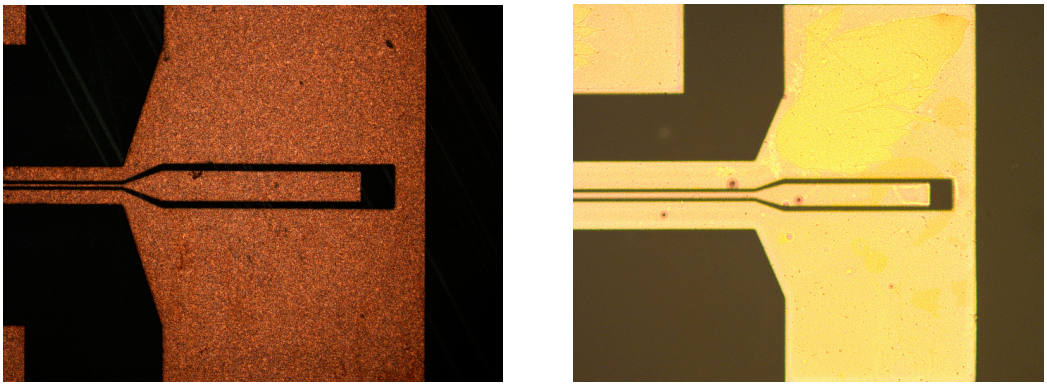


Figure 4.18: CPW with VNA probing pad on glass interposer etched by: standard spray etch (left) and differential etch (right)

All three different etching methods were tested and compared. Figure 4.17 shows the 5 μm line and space pattern after immersion seed layer etching and Atotech differential etching. The copper traces were badly deformed after immersion seed layer etching. Using differential etching, however, the line shape integrity was improved. Figure 4.18 shows the comparison between the two copper etchants. The copper surface became rougher and matte after applying a standard copper etchant, but the differential etchant was capable of yielding a shiny and smooth copper surface due to the increased etched selectivity between electroless and electrolytic plated copper.

Another technique to improve the yield and avoid over-etch is to add end-point detection to the etching system. Although such systems are commonly used in wafer fabrication, this research introduces such a concept to large panel processing to improve line width control and prevent over-etch. The spray etch tool was provided by Veeco Inc., with a camera on top of the sample to detect the end-point based on the color change of the sample. The major advantage of this technology is to avoid the seed layer over-etch that damages the copper structures and causes significant line width variations. Figure 4.19 shows the 5 μm comb structure and escape routing pattern after seed layer etch using isotropic etchant with end-point detection system. No seed layer residue and no copper traces lift-off due to over-etch was observed. Since the copper etchant applied is an isotropic etchant, the copper surface is relatively rough compared with the differential etching method. Furthermore, the end-point needs to be controlled carefully to avoid under-etch, leaving seed layer residues in some cases.

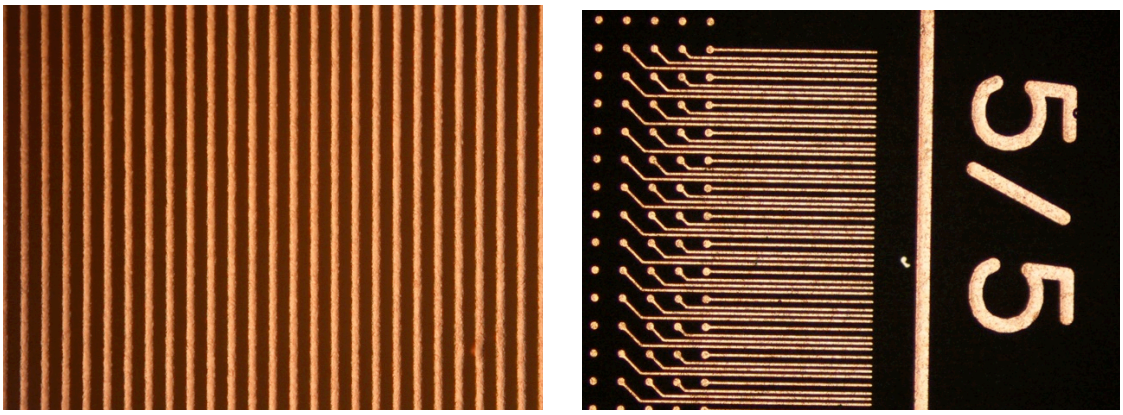


Figure 4.19: 5 µm comb structure and escape routing pattern after seed layer etch on the end-point detection system

The differential etch method was selected as the front-up seed layer etching method due to its advantages discussed above. Figure 4.20 shows the escape routing test pattern with 5 µm line and space on glass interposer after DFR strip, and Figure 4.21 shows the same structure after differential seed layer etching. No seed layer residue is observed from the image, and the etching process did not deform or alter the line shape significantly. Following SAP, open/short tests of this escape routing pattern confirmed that the improved seed layer etch process resulted in no seed layer residues. Test structures with 2 µm line and space escape routing patterns at 40 µm pad pitch were also fabricated on glass substrates using the same process, as shown in Figure 4.22. Optical inspection of this structure revealed approximately 0.5 µm side wall etch, resulting in 1 µm line width reduction. This demonstrates the limitation of etch selectivity of the improved SAP process at 2 um line and space and must be considered during interposer design to improve process yield. The actual line and space for 2 µm designed pattern was 0.8 µm line and 3.2 µm space (Figure 4.22). To further understand the side wall etch

amount for design compensation, a photo mask with multiple line widths and spaces was designed. The measured line width and space before and after seed layer etch is shown in Table 4.3. The thickness of electroless copper seed layer was 0.2 µm and the thickness of the copper traces was approximately 2 µm. The data in Table 4.3 was measured from the top views of optical microscope images, with a ±0.1 µm error margin. The average side wall etch amount was around 0.5 µm, resulting in 1 µm line width shrinkage. It was observed that the side wall etch amount slightly increases when the space increases. According the simulations in Section 3.4, 1 µm width decrease falls within 10% impedance tolerance of microstrip line for 7.5 µm width and above, but leads to 20% impedance increase for 2.94 µm stripline. Considering the wider DFR gap after ozone treatment, the overall line width change is around 0.5 µm or less, which satisfies the 10% impedance target for 2.94 µm stripline and 5% impedance target for 7.5 µm microstrip line. If more strict impedance tolerance is required, the mask design compensation needs to be carefully considered.

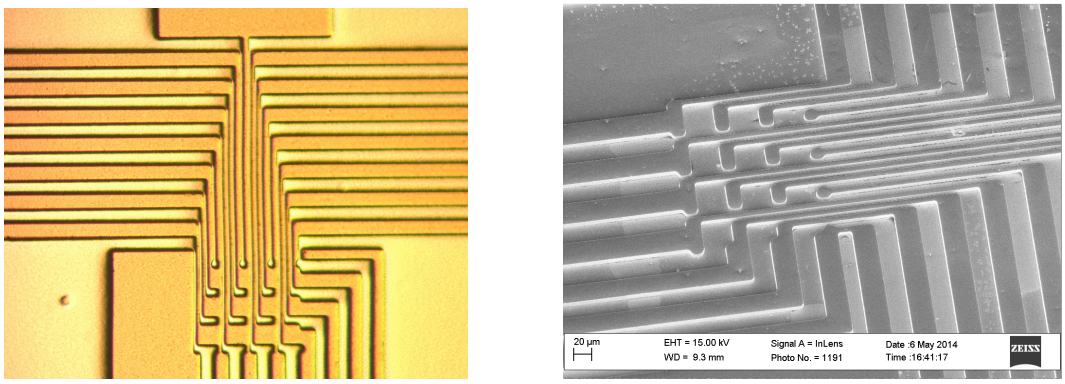


Figure 4.20: Optical microscope and SEM image of 5 µm line and space escape routing test patterns before copper seed layer etching

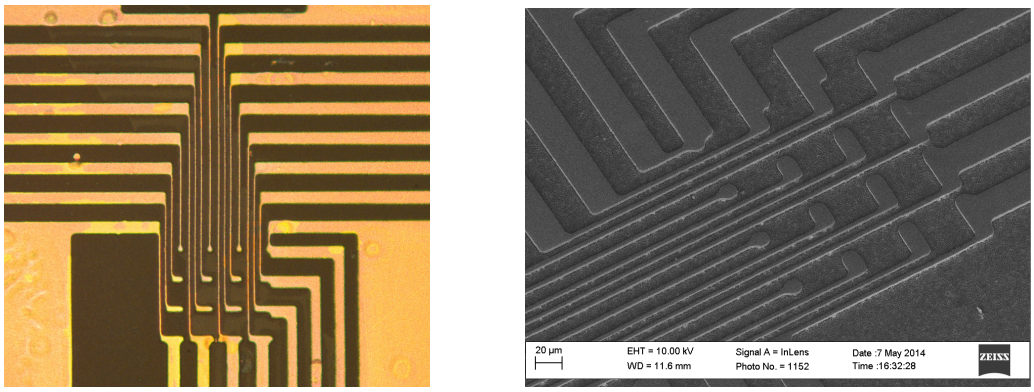


Figure 4.21: Optical microscope and SEM image of 5 µm line and space escape routing test patterns after copper seed layer differential etching

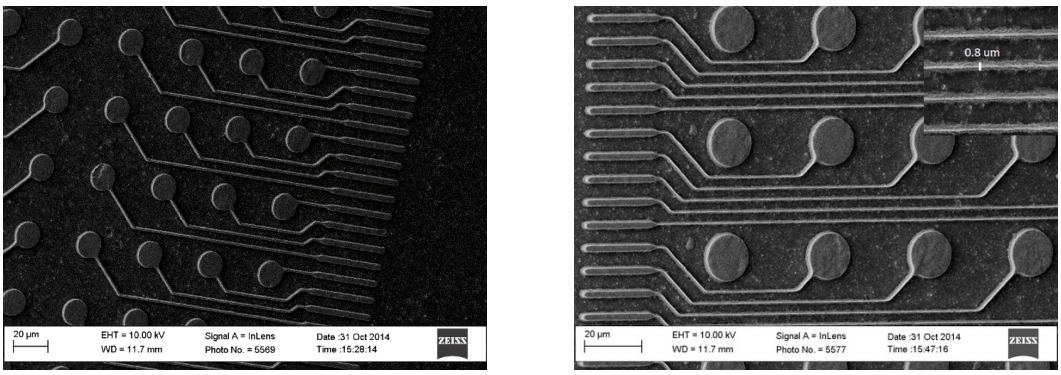


Figure 4.22: SEM image of 3 µm line and space (left) and 2 µm line and space (right) escape routing pattern at 40 µm pad pitch

Table 4.3: Measured copper line and space before and after seed layer etching

Line/Space before etch	2/2	2.1/2.9	2/4	2.3/4.7	2.8/3.2	2.8/4.2	2.7/5.3
Line/Space after etch	1.3/2.7	1.3/3.7	1.4/4.6	1.4/5.6	2/4	2.1/4.9	1.8/6.2
Line width shrinkage	**0.7**	**0.8**	**0.6**	**0.9**	**0.8**	**0.7**	**0.9**
Line/Space before etch	2.8/6.2	3.8/3.2	3.7/4.3	4/5	4/6	4/7	3.5/8.5
Line/Space after etch	2.1/6.9	2.9/4.1	3.1/4.9	3.1/5.9	3.1/6.9	3.1/7.9	2.5/9.5
Line width shrinkage	**0.7**	**0.9**	**0.6**	**0.9**	**0.9**	**0.9**	**1**
Line/Space before etch	4.7/3.3	4.9/4.1	4.9/5.1	4.9/6.1	5/7	5/8	5.1/9.9
Line/Space after etch	3.7/4.3	3.8/5.2	3.7/6.3	3.8/7.2	4/8	3.8/9.2	4/11
Line width shrinkage	**1**	**1.1**	**1.2**	**1.1**	**1**	**1.2**	**1.1**

Optimizing the electroless copper plating to obtain better seed layer thickness uniformity, and the seed layer etch conditions can improve fine line yield using the SAP

method. The copper seed layer was electroless plated on the polymer surface. Strong adhesion is required to ensure the fine copper traces do not delaminate from the polymer. Therefore, a desmear process was applied to the polymer surface before electroless copper plating, as discussed in Section 3.2.1. The surface roughness of polymer before and after the desmear process is shown in Figure 3.5. The increased R_z, however, plays a critical role in the copper seed layer etch process. The copper seed on a larger R_z surface has stronger adhesion but suffers from longer seed layer etch times, causing excessive and non-uniform undercut. The seed layer etch on the roughened polymer surface is shown in Figure 4.23. The initial seed layer etch rate is fast and independent of the polymer roughness. However, it is difficult to fully etch the copper seed layer residue that is embedded in the rough polymer sub-surface, thus requiring extended etching times. This causes a decrease in the overall seed layer etch rate and increases the amount of copper trace side wall lateral etch, resulting in lower yield of the fine copper traces. Therefore, proper optimization of copper to polymer adhesion using desmear and mask design compensation are needed to improve fine line yield.

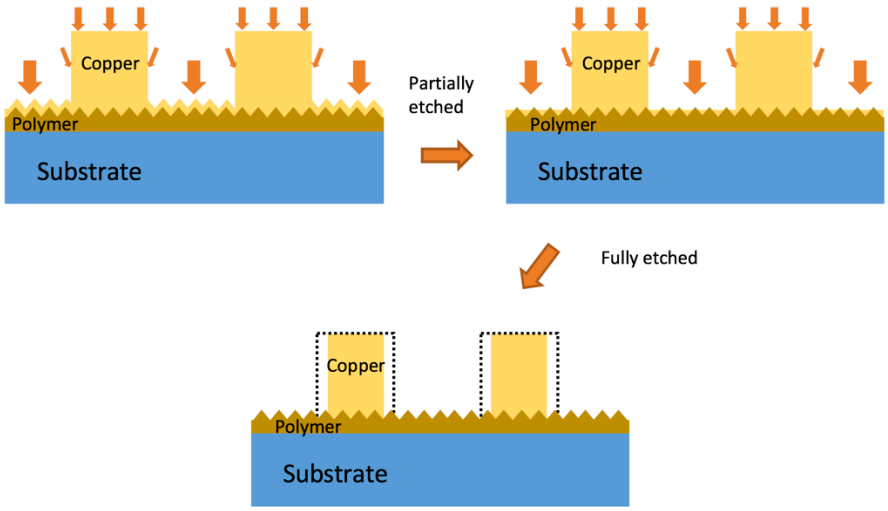


Figure 4.23: Copper traces side wall etch due to roughened polymer surface

4.5 Panel Scale Surface Planarization for Copper Thickness Control

As described in Chapter 3, any non-uniformity in the copper trace thickness results in dielectric thickness variations, leading to impedance changes that degrade signal integrity. During the electrolytic plating step, the plated copper thickness is dictated by the electrical current density, which is not constant across the whole panel due to variations in the RDL design. The current density on large patterns is usually lower than on fine patterns, resulting in lower copper thickness in low current density areas. An additional factor for ultra-fine patterns is the variation in the fluid exchange in small gaps. When the pattern size reduces to 2 μm and below, process chemicals could be trapped in the narrow trenches formed in the photoresist. This lower amount of fluid exchange could result in thinner copper structures than wider patterns, as shown in Figure 4.24. This uneven copper RDL manifests itself as polymer dielectric thickness non-uniformity, leading to poor co-planarity of the substrate and negatively affecting the yield of lithography process for next layer fabrication, as well as impacting the impedance uniformity across the panel.

Figure 4.24: Uneven copper thickness after electrolytic plating

A Chemical Mechanical Polishing (CMP) process is utilized for polishing and planarizing the copper surface during wafer level processing, but has not been scaled to large panel 2.5D glass or laminate interposers. In this research, a cost-effective thinning

and planarization method for ductile materials using a diamond cutter on a spindle was investigated. This method can be applied to metals such as Au, Cu, and solders, polymers including photoresists, epoxy dielectrics and underfills, and passivation layers such as BCB and polyimide. The kinematics of the planarization tool developed by Disco Japan, is shown in Figure 4.25 [42]. A single bit of diamond is mounted on a spindle which rotates at high speeds during the process. This spindle's height is fixed, while the chuck table where the sample is held is slowly fed under the diamond cutter. The parallelism between the chuck table surface and diamond cutter rotating plane was precisely controlled to ensure 1 µm co-planarity. The unevenness of the sample surface would be shaved by the rotating diamond cutter. Such a planarization process by diamond cutter is capable to planarize embedded as well as free-standing structures.

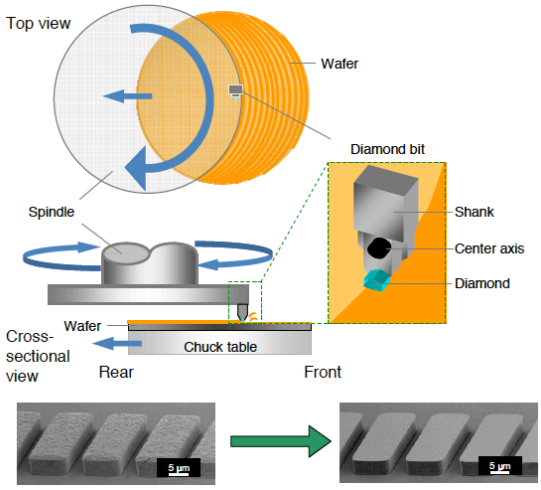


Figure 4.25: Kinematics of ductile materials' surface planarization with Au metal bumps as an example [42]

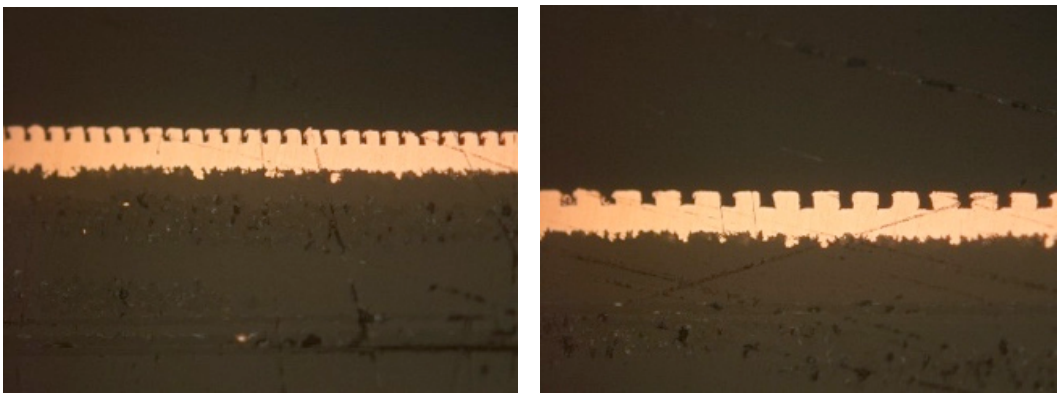


Figure 4.26: Free-standing copper comb structure after surface planarization. Cross-sectional view of 5 µm (left) and 10 µm (right) line and space

Copper clad laminate (CCL) test substrates were patterned by electrolytic copper plating for the preliminary tests. The DFR was stripped, leaving the free-standing copper structure to be planarized. The targeted copper pattern thickness was 5 µm. The cross-sectional image of the comb structure after planarization is shown in Figure 4.26. The fine copper traces were deformed during the planarization process, due to the shear force of the diamond bit cutting. The larger traces (10 µm) showed less signs of deformation. Therefore, for planarization of fine line RDL, a support layer was required to prevent copper deformation. The second planarization test sample was fabricated on a 300 µm thick glass panel using the advanced SAP method described earlier. The process flow of improved planarization process is shown in Figure 4.27. The DFR thickness was 7 µm and the copper was over-plated. The DFR acted as the support layer for fine copper patterns. After planarization, the DFR was stripped and the copper seed layer was etched in a spray etching tool using Atotech differential etchant. The cross-sectional images of the sample right after planarization and after seed layer etch are shown in Figure 4.28. No deformation of copper traces was observed. Another improvement of this planarization

process is that the copper surface roughness is greatly reduced after the diamond bit cutting. During the seed layer etch process, a smooth copper surface will result in less copper trace etching due to the smaller surface area, which further improves the SAP RDL yield in addition to the differential seed layer etching.

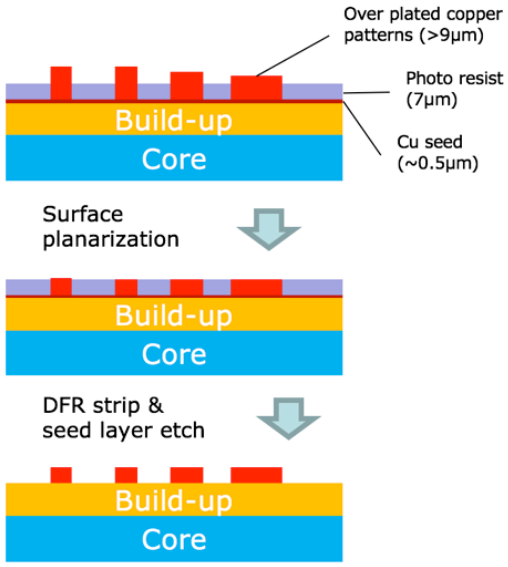


Figure 4.27: Modified copper surface planarization process flow

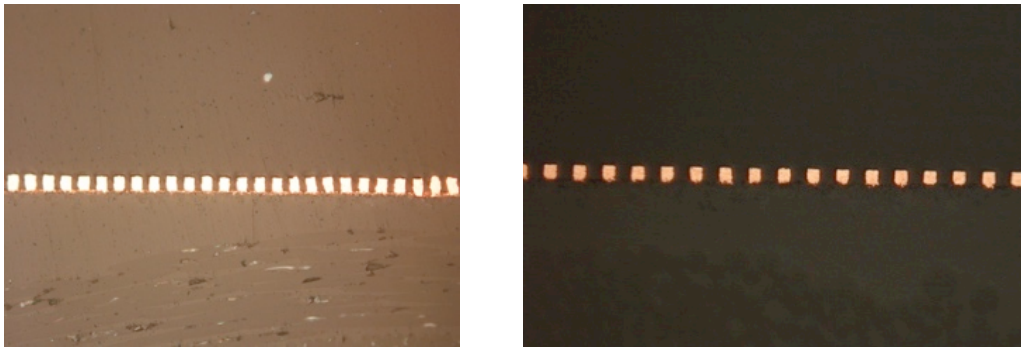


Figure 4.28: Cross-sectional view of 5 μm line and space copper traces after planarization with DFR and seed layer (left) and after DFR strip and seed layer etch (right)

If the effective dielectric thickness between different metal layers is critical for impedance control, this surface planarization process can be further modified to planarize the copper layer as well as the dielectric layer. This process flow is shown in Figure 4.29. The copper structure was embedded in the dielectric polymer instead of the DFR as in the previous planarization method. Since the seed layer was etched prior to the planarization, the smooth top surface of the copper structure was preserved. Figure 4.30 shows the top view of planarized escape routing patterns with 3 μm and 5 μm line and space protected by the polymer dielectric. After this step, another polymer layer was laminated on top of planarized metal layer, and thinned down to the desired thickness for impedance control with the same surface planer tool. Then the SAP method was repeated starting with seed layer deposition for a third metal layer fabrication. A three-metal-layer RDL structure with around 3 μm effective dielectric polymer thickness reduced from 5 μm ABF-GX92P was demonstrated with the above SAP process flow with surface planarization steps, as shown in Figure 4.31. The accuracy of the polymer thickness across the panel is determined by the surface planer tool system, and was less than 1 μm panel wide. This modified surface planarization process has the potential to achieve impedance controlled microstrip line designs where ultra-thin dielectric layers are required.

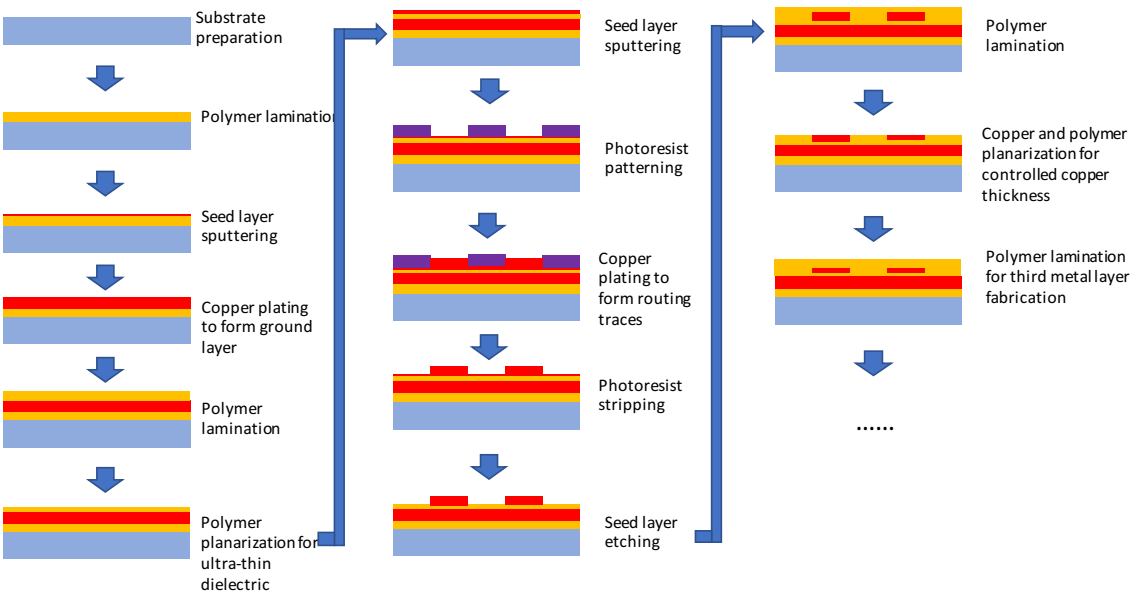


Figure 4.29: Modified surface planarization process flow. Both metal layer and polymer dielectric layer are planarized

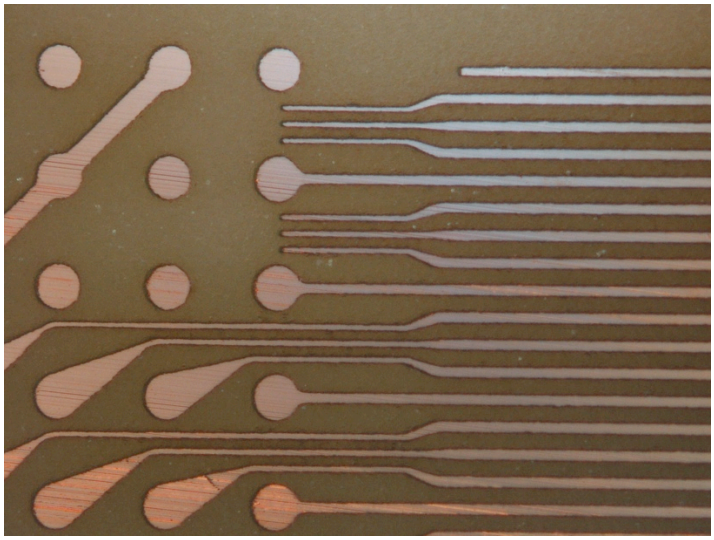


Figure 4.30: Top view of planarized escape routing patterns with 3 µm and 5 µm line and space protected by polymer dielectric

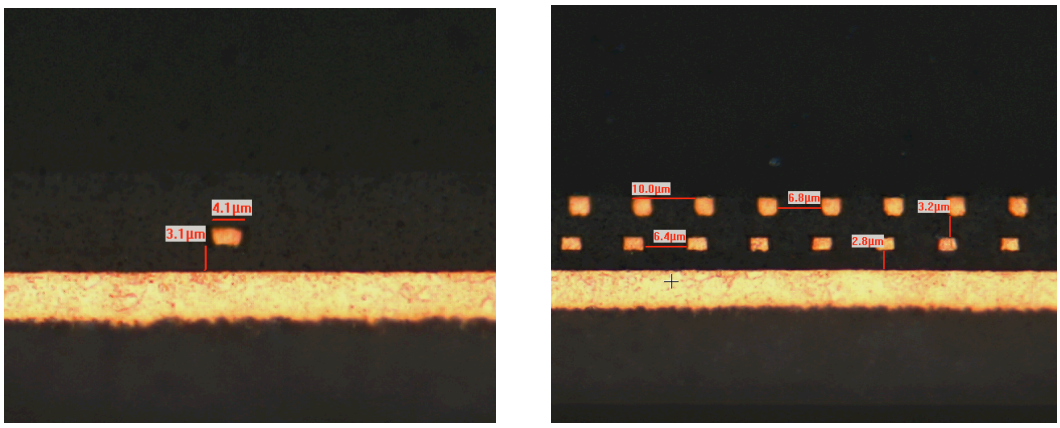


Figure 4.31: Cross-sectional view of 3 metal layer RDL with around 3 µm effective dielectric polymer thickness, fabricated by SAP method with surface planarization applied on both metal layer and dielectric layer

4.6 Summary

In this chapter, the traditional SAP method for multi-layer RDL fabrication was advanced to achieve 2 µm line and space high density routing, closing the gap in routing density between wafer foundries and package foundries.

The photo lithography process with DFR was optimized by enhancing the adhesion between the DFR and the copper seed layer, as well as by applying a thinner DFR with optimized projection lithography. The resolution was successfully advanced to 2 µm on DFR, enabling 2 µm panel compatible SAP processes.

An innovative ozone treatment was studied and implemented in the SAP method before electrolytic copper plating and after DFR stripping, as a higher throughput alternative to traditional oxygen plasma treatment. The ozone treatment cleans the organic contamination on the sample after lithography, and significantly improves the surface wettability, which is essential for high quality copper plating. The ozone

treatment etches a small amount (~0.6 μm on each side) of DFR, which needs to be considered for design compensation. Another application for the ozone treatment is cleaning the DFR residue after strip, for improving the overall yield of the SAP method.

Three different copper seed layer etching processes were compared and analyzed. The spray etching tool increases the vertical etching speed, while the differential etchant called EcoFlash from Atotech etches copper seed layers faster than the plated copper structure, leveraging the different copper grain structures. An etch tool with an end-point detection system provided a safe stop to avoid seed layer over-etch and potentially further reducing process variations. The spray etching method with differential etchant provided the best seed layer etch process control, with less side wall damage and a smooth copper structure after etch. The side wall etch amount was from 0.3 μm to 0.6 μm on each side, depending on the space between traces. Considering the ozone treatment impact on DFR, the overall line width change can be controlled within 0.5 μm. This width variation satisfies the 10% impedance target for 2.94 μm stripline and 5% impedance target for a 7.5 μm microstrip line. Design compensation needs to be considered for a stricter impedance target.

Lastly, a panel scale surface planarization process was optimized and demonstrated to achieve uniform copper thickness across the panel, eliminating the non-uniformity in copper and dielectric thickness after copper plating. Furthermore, the dielectric polymer layer can also be planarized to reduce its thickness for impedance control in ultra-fine lines.

CHAPTER 5

MILLIMETER-WAVE CHARACTERIZATION OF PHOTO-SENSITIVE DIELECTRIC AND DEMONSTRATION OF IMPEDANCE CONTROLLED TRANSMISSION LINES ON GLASS INTERPOSERS

In the previous two chapters, electrical modeling and advanced SAP processes for 2 μm RDL on glass interposers were investigated. Considering the design guidelines from Chapter 3 as well as the SAP advancement for 2 μm multi-layer RDL fabrication, this chapter discusses the electrical property extraction of new ultra-thin photo-sensitive dielectric material for via and trench formation, and transmission line characterization up to 40 GHz for electrical model correlation. The design and fabrication of an enhanced coupling ring resonator for characterizing photo-sensitive dielectric are discussed. High frequency electrical characterization results of fine transmission lines are presented and correlated with the electromagnetic simulation results. A simple and fast VNA landing pad deembedding algorithm was adopted for better simulation-to-measurement correlation. Finally, the design rule of 2 μm microstrip line is provided, and a 2 μm single copper trace is demonstrated with the width control within 5% by the advanced SAP process developed in Chapter 4.

5.1 Electrical Characterization of Photo-sensitive Dielectric Material by the Ring Resonator Method

The RDL process research described in the previous chapters was conducted on an epoxy polymer dielectric with a high percentage of ceramic particulate fillers for reducing the CTE of the material. Also, the dielectric used was non-photo sensitive, requiring laser ablation to form the layer to layer via interconnections. This process has traditionally been limited to via diameters above 5-10 μm. The emerging photo-sensitive dielectric materials, also known as photo-imageable dielectric (PID) materials have similar resolution to DFR, capable of forming vias in the 2-6 μm diameter range, as well as forming high density trenches for the embedded method discussed in Chapter 3. Besides the process development for such photo-sensitive dielectric films, the accurate characterization of electrical properties for impedance controlled design rules is also required. The electrical ring resonator method based on microstrip lines is one of the common ways to characterize the dielectric permittivity and the loss tangent [43]. The microstrip line based ring can be modeled as two straight sections of microstrip lines connected in parallel. The ring resonates when the mean ring circumference (l)

$$l = n \times \lambda \ \ (n = 1,2,3,\cdots) \tag{5.1}$$

where λ is the wave length of the electromagnetic wave that propagates in the microstrip ring. The mean ring circumference is the average value of the inner ring circumference and the outer ring circumference. The impedance control of the microstrip lines for the ring resonator is not critical. However, to minimize the return loss of the feed line, the feed line and the ring were designed at 50-ohm impedance. The estimated relative dielectric constant of the thin-film photo-sensitive dielectric material provided by TOK

was 3.2, and its thickness was 20 μm. According to the simulation result of the 2D extractor model, the width of the 50-ohm microstrip line was 43 μm with copper thickness of 4 μm.

To complete the ring resonator design and estimate its coupling strength, a full wave 3D HFSS model was created with tunable parameters and simulated to find a proper ring diameter to achieve the first-order frequency at 5 GHz. The ordinary ring model and one of its line-to-ring coupling structures is shown in Figure 5.1. The tuned mean ring radius was 5.2 mm and the coupling gap was 10 μm. The first resonance occurred at 5 GHz as targeted. However, the width of the microstrip feed line was too narrow to create a strong enough capacitive coupling. An enhanced coupling method was required to strengthen the capacitive coupling and ensure that the insertion loss of the ring resonator can be correctly measured by the VNA at resonant frequencies. The coupling enhanced ring resonator model and its zoomed in coupling structure are shown in Figure 5.2. Due to the modified tight coupling structure, the mean ring radius was increased to 5.4 mm to achieve 5 GHz first-order resonance. The simulated insertion loss of both the original ring resonator and the coupling enhanced ring resonator are shown in Figure 5.3. According to the result, the enhanced coupling method significantly reduced the insertion loss at the resonant frequency, making accurate VNA measurements possible.

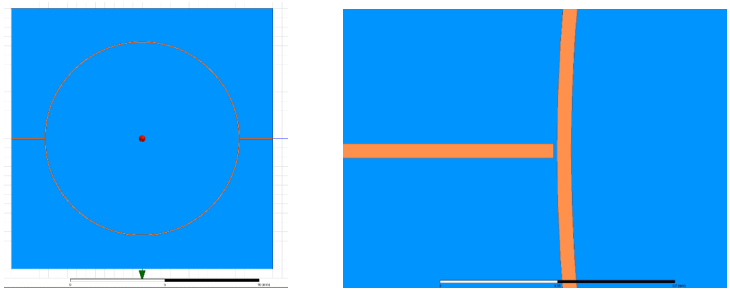


Figure 5.1: The top view of ordinary 5 GHz ring resonator HFSS model (left) and zoomed in line-to-ring coupling (right)

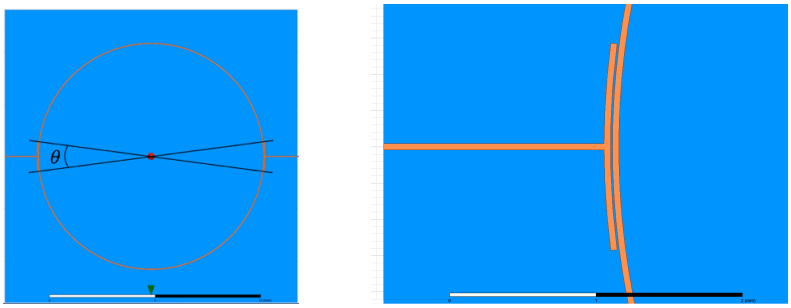


Figure 5.2: The top view of coupling enhanced 5 GHz ring resonator HFSS model (left) and zoomed in line-to-ring coupling (right)

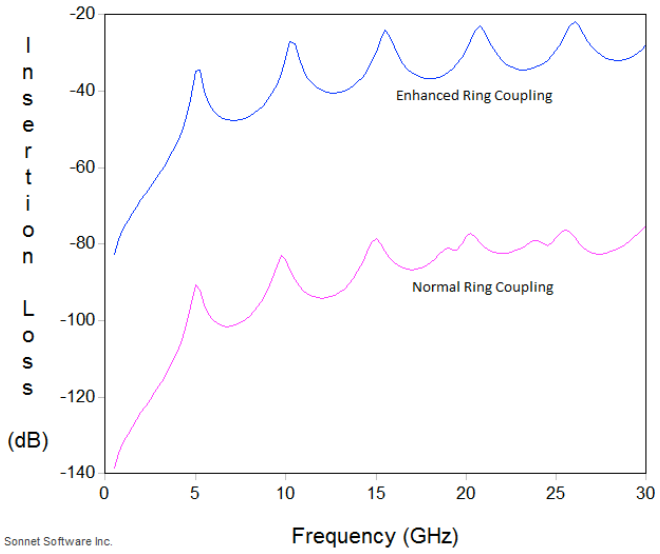


Figure 5.3: The insertion loss of both ordinary ring resonator and coupling enhanced ring resonator

Table 5.1: Designed parameters of coupling enhanced ring resonators for the characterization of photo-sensitive dielectric material

First-order resonate frequency	Polymer thickness	Copper thickness	Copper trace width	Mean ring radiation	Coupling gap	Tight coupling angle (θ)	Occupied area
5 GHz	20 μm	4 μm	43 μm	5.4 mm	15 μm	15°	14x14 mm^2
10 GHz	20 μm	4 μm	43 μm	2.8 mm	15 μm	15°	7x7 mm^2
15 GHz	20 μm	4 μm	43 μm	1.87 mm	15 μm	15°	5x5 mm^2

Three different size of coupling enhanced ring resonators were designed. The major parameters for these resonators are shown in Table 5.1, and an overview of mask design for the Ushio projection mask aligner is shown in Figure 5.4. The advanced SAP method was modified to fit the photo via formation process, as shown in Figure 5.5. The substrate selection has no impact on the measurement since the bottom ground metal layer shields the substrate from the electromagnetic field. After the ground plane was formed by electrolytic copper plating, a layer of photo-sensitive dielectric material with the required thickness was laminated. Then, the photo-vias were formed by a lithographic process with the designed via mask, for the electrical connections from the measurement pads to the ground plane. The dielectric material with vias was then cured and the copper seed layer was deposited by PVD sputtering, since the current generation high-resolution photo-sensitive dielectric is not compatible with direct electroless copper deposition. The DFR was laminated on the copper seed layer and patterned by a lithographic process. The ring structures were metallized by electrolytic plating, and the seed layer was etched after the DFR strip. In addition to the differential copper seed layer etching step, the thin titanium layer under the copper seed layer used as adhesion promoter was etched by TOK's titanium etchant. The final ring resonator structures were obtained after the titanium etching.

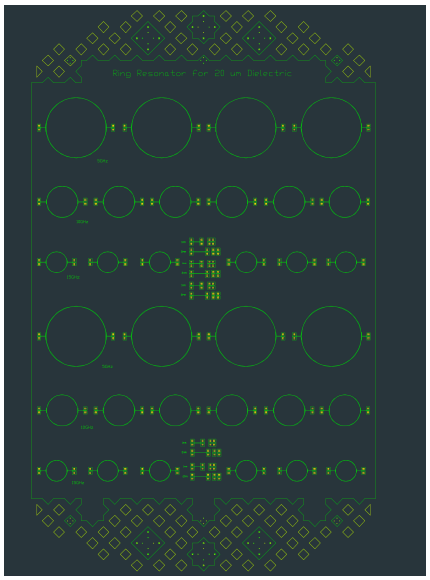


Figure 5.4: The photo mask design containing 3 sizes of ring resonators and short microstrip lines

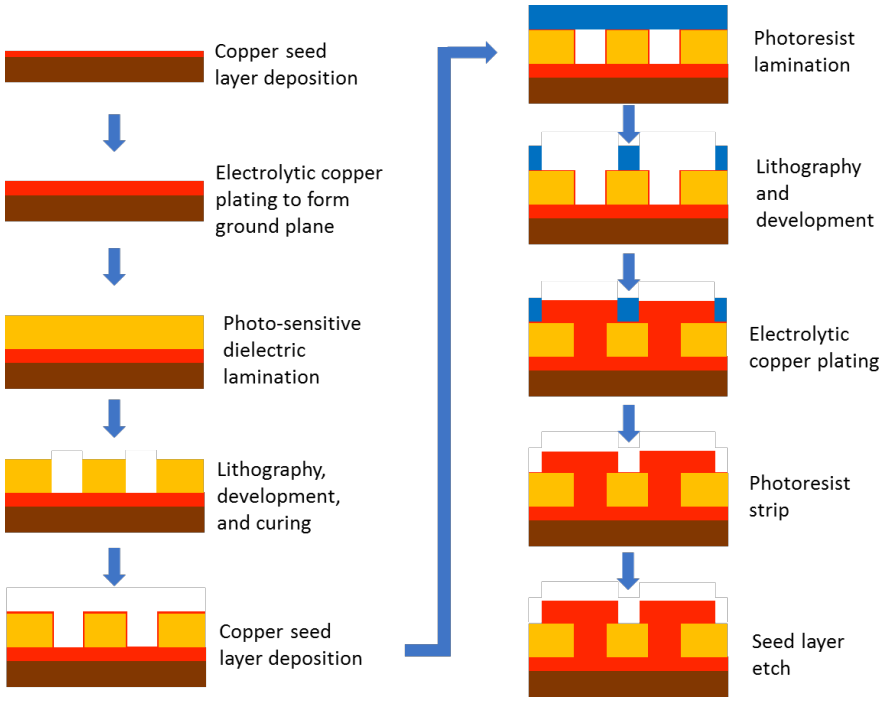


Figure 5.5: Modified SAP flow for ring resonator fabrication with photo-sensitive dielectric material

A simple and fast method to extract material electrical property from the VNA measurement was proposed by modifying HFSS model. The extraction flow chart is shown in Figure 5.6. Based on the material properties that TOK provided, the initial dielectric constant was set at 3.2, with a loss tangent of 0.01. The dimensions of fabricated ring resonators were measured and input into the HFSS model as well. The simulated insertion loss was compared to the measurement data. If the simulated resonance frequency matches well with the measurement, then the dielectric constant data was extracted from the HFSS model. If not, the material properties were adjusted in the HFSS model to re-simulate and compare to the measurements, and this process was repeated until the two resonant frequencies matched. The bandwidth at the resonance frequency was also compared, for the loss tangent extraction. Around each resonance frequency, the "sharpness" of the simulated insertion loss needs to be matched with the measurement data. When both simulated resonance frequency and the corresponding bandwidth are matched well with measurement data, the material property in the HFSS model is the correct one and can be extracted. Since the ring resonator applied in this study had tight coupling between the feed line and the ring itself, the traditional equations for material property calculation were no longer accurate. 3D EM modeling was the only method to accurately capture the tight coupling effect, and the simulation time was around 20 mins for a six-core Intel Core i7 PC with delta-S set as 0.5%. Therefore, this method is significantly more accurate than equation based calculations and efficient enough for material property extraction.

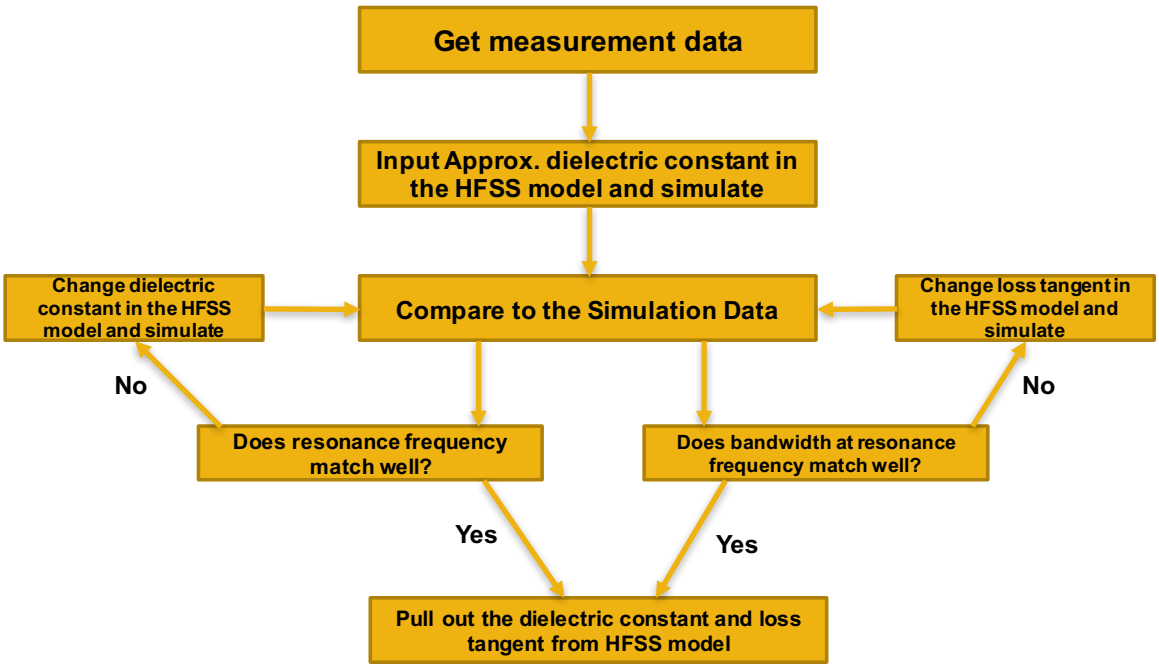
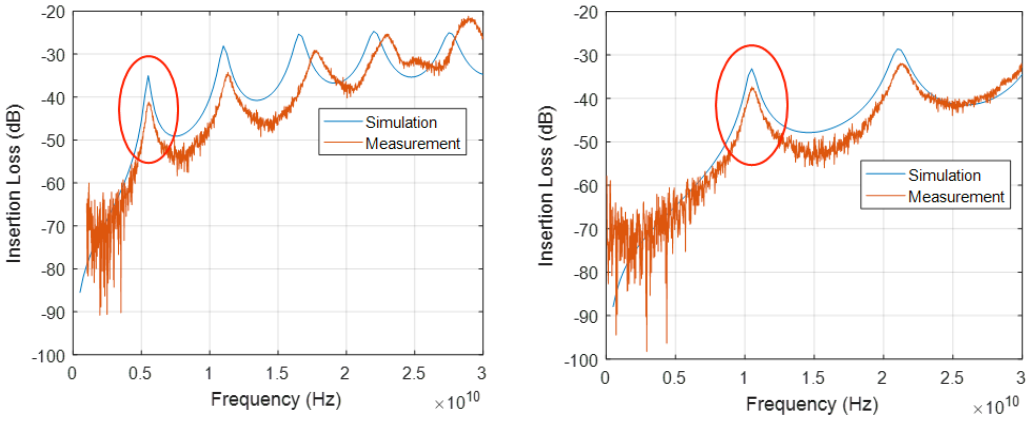
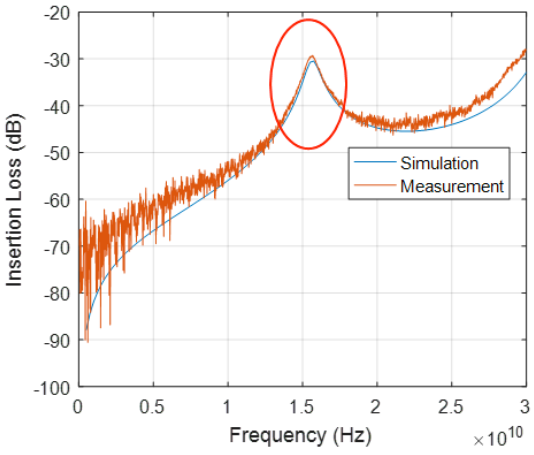


Figure 5.6: Material electrical property extraction from the measurement-to-simulation correlation

The measured insertion loss with correlated simulation results are shown in Figure 5.7. Only the first resonance frequency of each ring resonator was correlated with the HFSS model. Both the simulated resonance frequency and corresponding bandwidth matched well with measurement data, as highlighted in Figure 5.7. The extracted IF series photo-sensitive dielectric material property from TOK is shown in Table 5.2. It can be noted that when frequency increases, the loss tangent starts to increase significantly, which is expected since this dielectric polymer does not contain silica fillers. Therefore, the potential applications for current generation photo-sensitive dielectric polymers are at relatively lower frequency but ultra-high density routing using the embedded photo trench method allows one to achieve overall high signal bandwidth for interconnections.



(a) **(b)**



(c)

Figure 5.7: Correlated simulation and measurement results of ring resonators for material property extraction: (a) 5 GHz ring, (b) 10 GHz ring, and (c) 15 GHz ring

Table 5.2: Extracted relative dielectric constant and loss tangent of IF series photo-sensitive dielectric material from TOK

Measured frequency	Relative dielectric constant (Dk)	Loss tangent (Df)
5.5 GHz	3.1	0.02
10.5 GHz	3.1	0.03
15.7 GHz	3.2	0.04

5.2 Characterization of Transmission Lines on Glass Interposer

In this section, CPW and microstrip transmission lines were designed and fabricated on a polymer laminated glass substrate using the advanced SAP method. The fabricated transmission lines were measured by a VNA (Agilent 8510C) calibrated to 20 GHz using the SOLT method. The measurement results were analyzed comparing to the simulation results. The VNA probe landing pad effect was analyzed by the HFSS model simulation. Figure 5.8 shows two CPW transmission line HFSS models with and without VNA probe landing pads, and Figure 5.9 shows the simulated return loss and insertion loss. According to the simulation results, the VNA probe landing pads add a small fraction of the transmission line electrical length, which affect the return loss resonant frequency, and slightly increase the insertion loss by an insignificant 0.1 dB up to 30 GHz. Therefore, the VNA pads were omitted in the CPW and microstrip models for faster processing time without sacrificing too much accuracy.

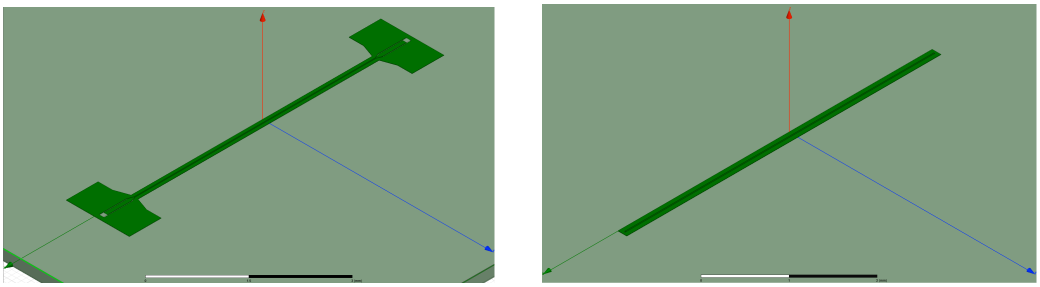


Figure 5.8: CPW HFSS model with VNA probe landing pads (left) and without VNA probe landing pads (right)

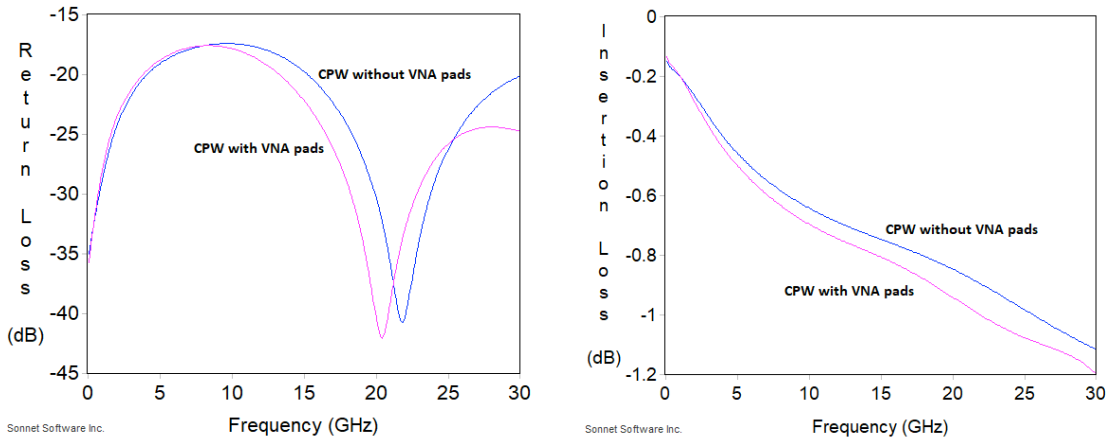


Figure 5.9: Simulated insertion loss and return loss of CPW with and without VNA probe landing pads

5.2.1 CPW Fabrication and Characterization

A single metal layer CPW structure was designed with 50-ohm impedance and fabricated on a polymer laminated glass substrate using the advanced SAP method discussed in Chapter 4. The low loss dielectric polymer thickness was 17.5 µm with a dielectric constant of 3 and a loss tangent of 0.005. The fabricated CPW had slightly different dimensions than designed due to various process variations discussed in Chapter 3. The targeted 50 Ω impedance CPW had a 10 µm width signal line, a 6 µm signal to ground gap, a 60 µm width ground trace, and a 6 µm copper thickness. The seed layer etch step etched roughly 0.5 µm copper. After fabrication, the final measured signal width was 9.04 µm, the gap was 7.14 µm, the ground trace width was 59.33 µm, and the copper thickness was 5.5 µm, as shown in Table 5.3. The length of the CPW excluding the VNA probe landing pad was 5 mm. Part of the fabricated CPW with one probe landing pad is shown in Figure 5.10. The fabricated CPW was measured by a VNA calibrated to 20 GHz using the SOLT method.

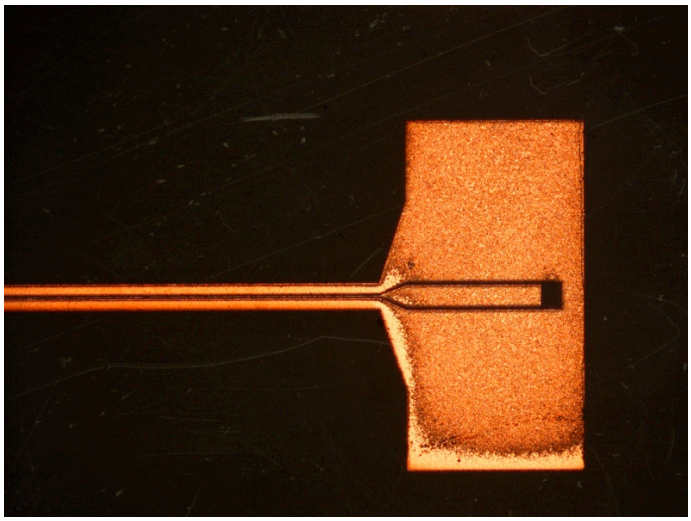


Figure 5.10: Part of the fabricated long CPW with one VNA probe landing pad

Table 5.3: Designed and fabricated parameters of CPW

CPW	Designed Value	Fabricated Value
Copper thickness	6 µm	5.5 µm
Signal trace width	10 µm	9.04 µm
Signal to ground gap	6 µm	7.14 µm
Ground trace width	60 µm	59.33 µm
Copper to polymer interface roughness (R_a)	N/A	0.1 µm
Copper surface roughness (R_a)	N/A	0.2 µm

The 3D HFSS model with wave excitation ports and driven terminal mode was made to simulate the return loss and insertion loss of the original design and the fabricated sample with process variation for comparison. The process variation model included the width and thickness discrepancy to the original design as well as the copper surface roughness and copper-to-polymer interface roughness. The copper side wall taper angle effect was not considered. The simulation and measurement results are shown in Figure 5.11. For the return loss, the simulated result with both line shape variation and copper surface roughness showed better correlation with measurement than an ideal CPW and line shape variation only model. However, at frequencies higher than 15 GHz, the

discrepancy between the simulation and measurement is larger than expected. The main reason is the omitted VNA pads and the calibration error at high frequency. The VNA pads increase the electrical length of the CPW and shift the resonant frequency, and the VNA is difficult to calibrate over a wide frequency range, especially at high frequency. For the insertion loss, at low frequency range (<8 GHz), the surface roughness boundary condition over-estimated the conductivity loss, resulting in higher insertion loss than the model without surface roughness boundary condition and actual measurement. When frequency increased to 10 GHz and above, the model with surface roughness shows better correlation to the measurement result. However, nearly 0.4 dB discrepancy is present between simulation and measurement. It is plausible that the dielectric material has an increased loss tangent at high frequency range that is unknown to us and not captured in the HFSS model.

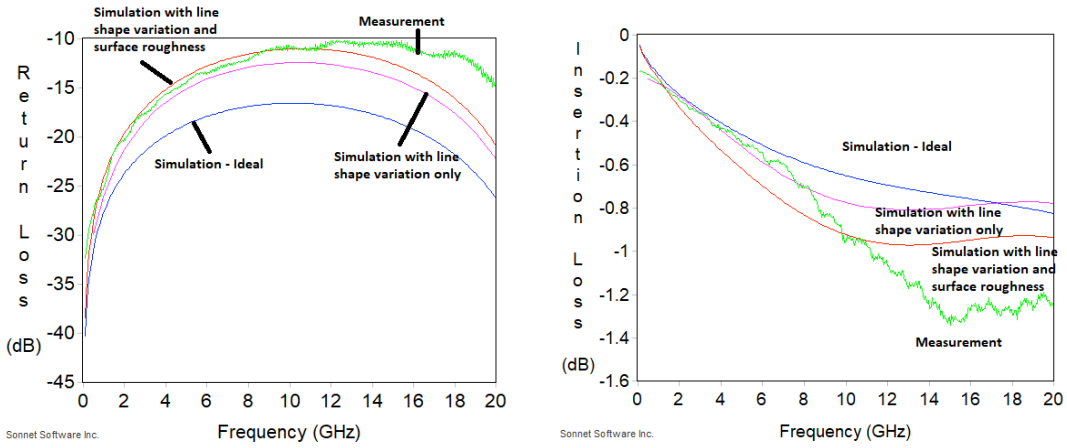


Figure 5.11: The simulated and measured S-parameters of 5 mm long single layer CPW on glass substrate

Another CPW with wider and thicker design was fabricated by the same advanced SAP method. The cross-sectional image of measured CPW line is shown in Figure 5.12.

A 5 µm thick nickel layer was deposited on the CPW surface to protect the copper trace during micro-section polishing. According to the fabricated transmission line dimensions, the CPW model in HFSS was modified to reflect the inclined copper trace sidewall (Figure 5.12). The measured and simulated insertion loss of the CPW on glass with a line width of 13.6 µm on top, 15.1 µm on bottom, 6.6 µm gap on top, 5.5 µm gap on bottom, and 5 mm length is shown in Figure 5.13. The surface roughness effect was also considered in the model. The two results correlate well with only around 0.1 dB differential. Considering the omitted VNA measuring pad in the HFSS model, the well correlated model-to-hardware result validates performance metrics obtained using the 3D HFSS model.

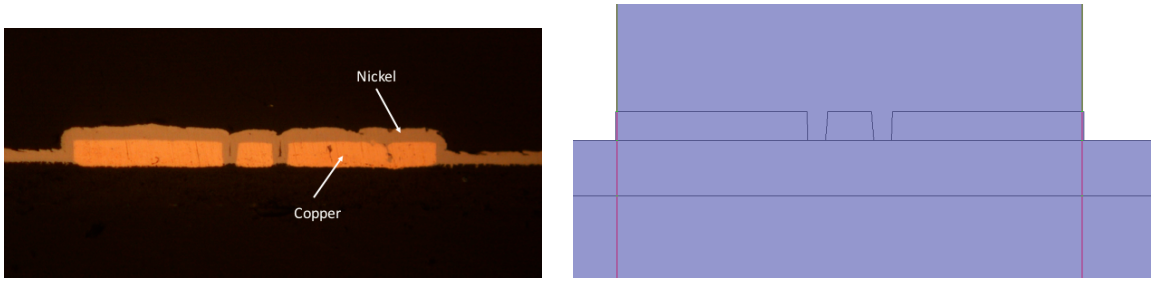


Figure 5.12: The cross-sectional image of fabricated CPW line (left) and the cross-sectional image of modified CPW model in HFSS with wave ports (right)

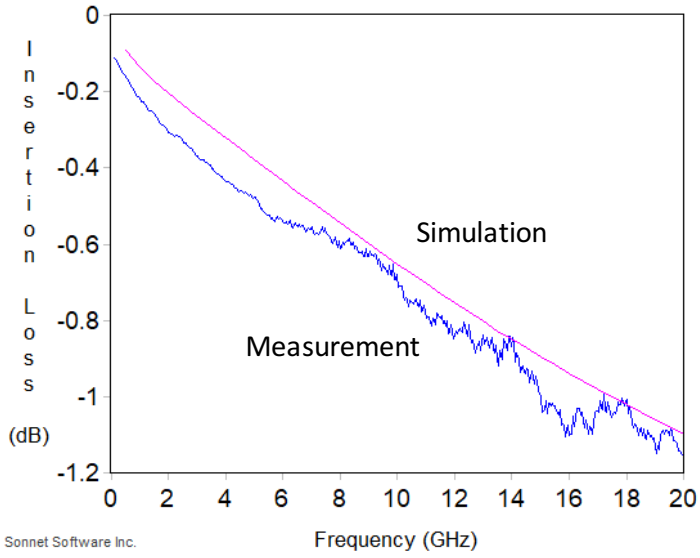


Figure 5.13: Simulated and measured insertion loss of CPW on glass interposer with tapered line width and gap at 5 mm length

To compare the glass interposer performance with silicon, the CPW transmission lines with same designs and build-up layers were also fabricated on a silicon wafer with polymer dielectric instead of thin silicon dioxide and measured with the VNA. The silicon wafer has the measured resistivity of 0.14 Ω•cm. The insertion loss of CPW on silicon is close to that on a glass interposer at low frequency, and the discrepancy becomes larger at high frequency, as shown in Figure 5.14. The silicon interposer requires a thicker dielectric layer than a glass interposer to achieve the same insertion loss, which leads to a larger total thickness of the silicon interposer. Therefore, glass, as an interposer material, is a superior alternative to silicon to improve high frequency electrical performance.

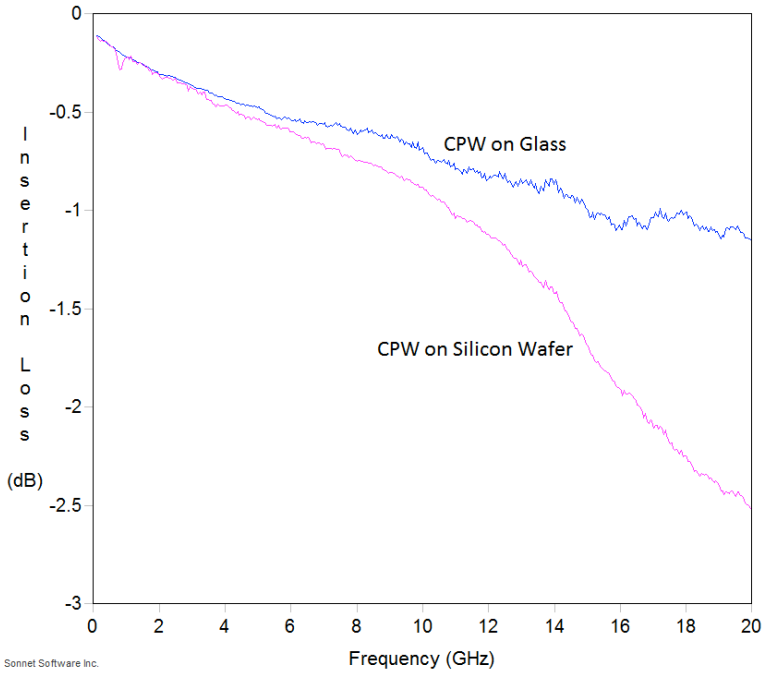


Figure 5.14: Insertion loss of CPW on glass and on silicon, with 13.6 µm line width, 6.6 µm gap, and 5 mm length

5.2.2 Microstrip Line Fabrication and Characterization

The microstrip line structure requires micro-vias for connecting the reference metal layer to the VNA probe landing pads. One simple method to form these micro-vias is by utilizing photo-sensitive dielectric material. The IF series photo-sensitive dielectric dry film polymer which was still under development by TOK was applied for this study. The extracted relative dielectric constant of this material is 3.1 with loss tangent of 0.03 at 10.5 GHz, according to Section 5.1. This polymer film is not compatible with the required desmear process for electroless copper deposition process. As a result, PVD sputtered Ti/Cu seed layer was employed instead. The designed and fabricated microstrip line parameters are shown in Table 5.4. The length is 2 mm length excluding VNA pads. Without the desmear process, the copper to polymer interface is very smooth. The actual

effective dielectric thickness was 8 μm, which is measured from the cross-sectional view of the sample. The flowability of the current photo-sensitive polymer is lower than ABF, resulting in a higher-than-expected effective dielectric thickness.

The simulated and measured insertion loss are shown in Figure 5.15. Similar to the CPW characterization, the HFSS model with process variations shows better correlation to the measurement than the ideal model. At high frequency (>12 GHz), the discrepancy between simulation and measurement increases dramatically with frequency. The possible explanation is increased leakage current between signal and return pass at high frequency. One well-known disadvantage of the photo-sensitive dielectric material is its relative high loss tangent due to lack of filler inside the polymer. Therefore, when frequency increases, the loss tangent may increase significantly. At current status, the photo material is suitable for high density yet low frequency applications. The material companies are improving the photo materials for better electrical performance, which expands the applicability.

Table 5.4: Designed and fabricated parameters of microstrip line

Microstrip line	Designed Value	Fabricated Value
Copper thickness	5 μm	3.6 μm
Signal trace width	10 μm	8.2 μm
Dielectric thickness	5 μm	8 μm
Copper to polymer interface roughness (R_a)	N/A	0.035 μm
Copper surface roughness (R_a)	N/A	0.16 μm

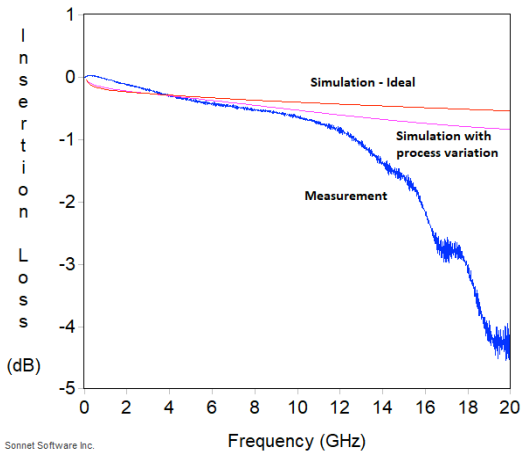


Figure 5.15: The simulated and measured insertion loss of microstrip line on glass substrate

5.2.3 VNA Probe Landing Pad Deembedding

The VNA probe landing pads on the transmission line test structure introduce a minor discrepancy the S-parameter compared to the model without the VNA pads. This section describes a simple method to deembed the VNA pads on a long transmission line with a shorter one using Matlab's RF toolbox. The two transmission lines have the same line dimensions and VNA pad designs, except the length. The procedures are described below:

1. Measure the S-parameters of both short and long transmission lines;

2. Divide the S-parameter of short transmission line into two equal ones, called S-parameter bi-section;

3. Deembed the long transmission line with the bi-sectioned S-parameter obtained in the previous step.

After deembedding, the effective length of the transmission line is the difference between the short and long transmission lines. The S-parameter bi-section algorithm in

Step 2 is to transform the S-parameter into an ABCD matrix, get the square root of this ABCD matrix and set it as a new ABCD matrix, then transform this new ABCD matrix back to a S-parameter. Figure 5.16 shows the flow chart to obtain the bi-sectioned S-parameter for the short transmission line. Matlab's RF toolbox also provides a simple function to deembed a measured S-parameter with two other S-parameters, called "deembedsparams". With the S-parameter of the long transmission line (S-parameter to be deembedded) and two equal bi-sectioned S-parameters, the deembedded S-parameters can be easily calculated with the above function. The S-parameter to be deembedded equals to the two bi-sectioned S-parameters and the deembedded S-parameter cascading together, as shown in Figure 5.17.

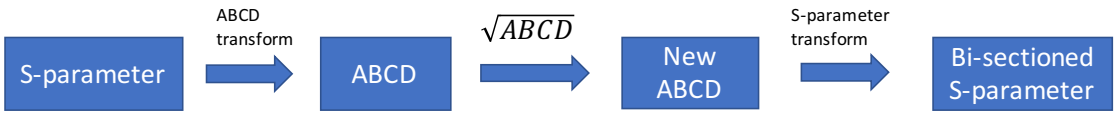


Figure 5.16: The flow chart to obtain bi-sectioned S-parameter

Figure 5.17: The relations of S-parameter to be deembed, bi-sectioned S-parameter, and deembedded S-parameter

The major drawback of this method is at frequencies when the S-parameter of the short transmission line has a phase shift from -180° to +180°, the huge error can occur around that frequency after bi-sectioning. Figure 5.18 shows the insertion loss of CPW with 5 mm effective length obtained by deembedding a 15 mm long CPW with a 10 mm

long CPW. Both CPWs have a width of 17.9 µm, signal to ground gap of 7.6 µm, and copper thickness of 5.5 µm. The insertion loss of the 10 mm long CPW has the phase shift from -180° to +180° at 10 GHz. As a result, the deembedded S-parameter matches well with HFSS model simulation except at the frequencies near 10 GHz.

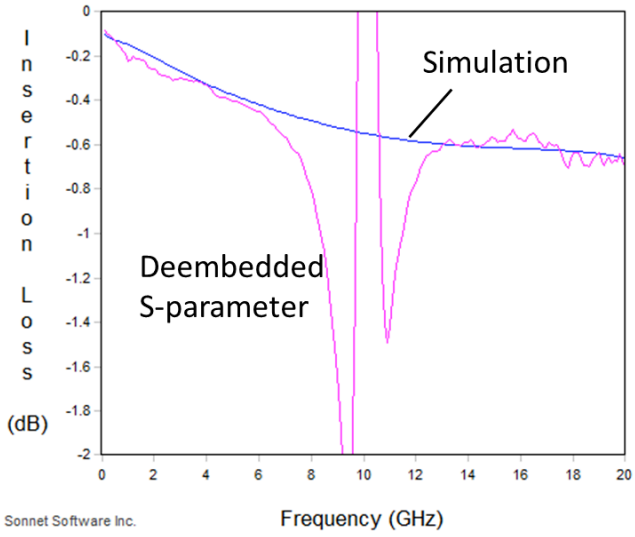


Figure 5.18: Insertion loss correlation of deembedded S-parameter to the simulation for 5 mm long CPW with 17.9 µm width, 7.6 µm signal to ground gap, and 5.5 µm thickness

However, this inaccuracy can be avoided by reducing the length of the short transmission line, to eliminate the phase shift from -180° to +180°. Figure 5.19 shows both the insertion loss and return loss of CPW with a 14.34 mm effective length obtained by deembedding a 15 mm long CPW with a 0.66 mm long CPW. The signal width of the CPW is 19.3 µm, the gap is 12.6 µm, and the thickness is 4 µm. Since the short transmission line is short enough to avoid the phase shift, the error caused by the S-parameter bi-section can be completely eliminated. It can be noted that the impedance

was not well controlled due to copper under-plating, resulting in thinner copper than designed which leads to higher impedance.

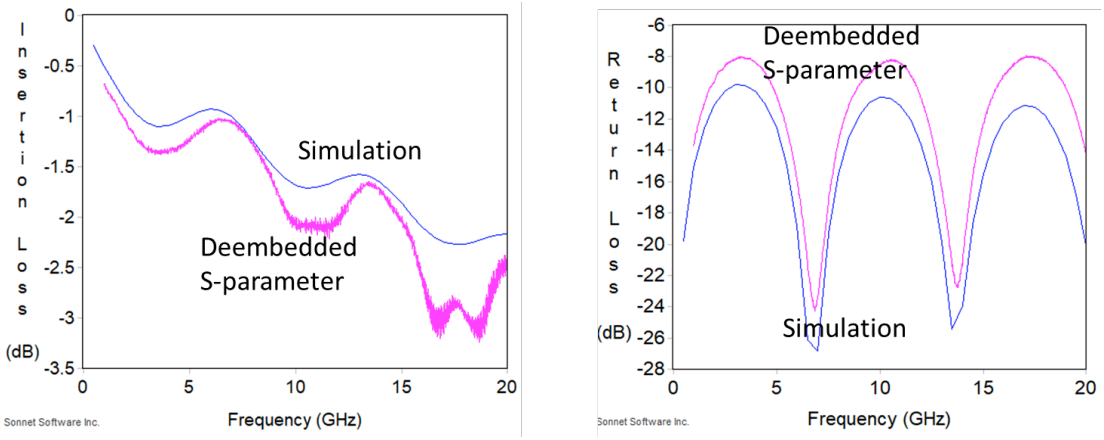


Figure 5.19: Insertion loss and return loss correlation of deembedded S-parameter to the simulation for 14.34 mm long CPW with 19.3 µm width, 12.6 µm signal to ground gap, and 4 µm thickness. The impedance was not well controlled due to thinner than expected copper

5.3 Design Rule for 2 µm Impedance Controlled Microstrip Line and Process Demonstration

In Chapter 3, a 2 µm wide microstrip line design parameters on a glass interposer with the ultra-thin dielectric was provided in Table 3.1. The proposed SAP method with the surface planarization process can separate the effective polymer thickness control from the copper thickness. With the same 2D extractor model applied in Section 3.4, the process variation sensitivity for a 2 µm microstrip line was calculated, as shown in Table 5.5. Only the two most sensitive process variations, which are the copper trace width and the thickness, were considered. Since the polymer thickness can be controlled individually by the surface planarization process, this thickness variation was also

included in the 2 μm design rule. According to the simulation results, the polymer thickness is the most critical parameter to keep certain impedance target, which is less than ± 0.1 μm for the 5% impedance tolerance. The copper trace width requires process controll within ±0.2 μm for the same impedance tolerance, and the copper thickness is much less sensitive.

Table 5.5: Calculated 2 μm microstrip line design rule with different impedance tolerance

		Width variation		Copper thickness variation		Polymer thickness variation	
Characteristic impedance (Ohm)	Percentage change	Trace width (μm)	Percentage change	Trace thickness (μm)	Percentage change	Polymer thickness (μm)	Percentage change
50	0	2	0	2	0	0.653	0
50.5	+1%	1.959	-2.05%	1.843	-7.85%	0.671	+2.76%
52.5	+5%	1.810	-9.5%	1.394	-30.3%	0.74	+13.32%
55	+10%	1.644	-17.8%	1.081	-45.95%	0.83	+27.1%
49.5	-1%	2.038	+1.9%	2.154	+7.7%	0.638	-2.3%
47.5	-5%	2.206	+10.3%	2.976	+48.8%	0.576	-11.79%
45	-10%	2.443	+22.15%	4.482	+124.1%	0.504	-22.82%

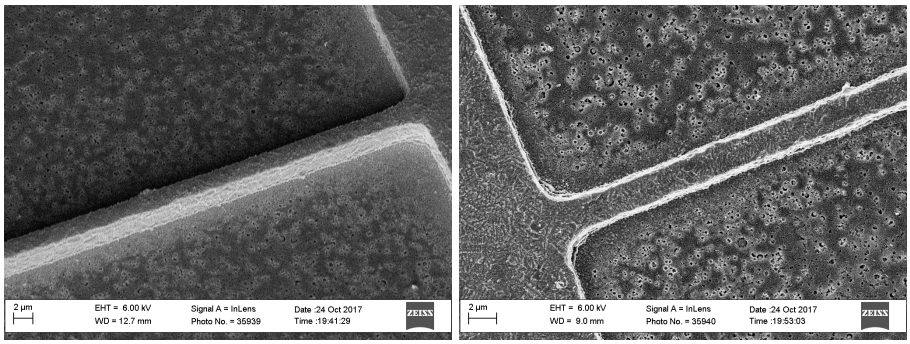


Figure 5.20: Tilted view (left) and top view (right) of a single 2 μm copper trace on polymer with actually measured width of 2.1 μm

With the design compensation, a 2 μm wide single copper trace was successfully fabricated on a polymer by the advanced SAP method, as shown in Figure 5.20. The

measured copper trace width is 2.1 μm, which is within 5% impedance target. However, the ultra-thin polymer is not available yet and requires future work.

5.4 Summary

This chapter demonstrates the coupling enhanced electrical ring resonator method to characterize the novel photo-sensitive dielectric material from TOK, and the transmission line characterization on a glass interposer compared with that on a silicon wafer, as well as a simple deembedding method to eliminate VNA probe landing pad impact.

Three coupling enhanced ring resonators with different first-order resonant frequencies were designed for TOK's photo-sensitive dielectric material. The ring resonators were fabricated by the advanced SAP method and measured by a VNA. An accurate and efficient method to extract dielectric constant and loss tangent by using a 3D HFSS model was proposed and demonstrated with measured insertion loss of ring resonators. The extracted TOK's IF series photo-sensitive dielectric material relative dielectric constant is 3.1 @5.5 GHz, 3.1 @10.5 GHz, and 3.2 @15.7 GHz. The loss tangent is 0.02 @5.5 GHz, 0.03 @10.5 GHz, and 0.04 @15.7 GHz.

The transmission line test structures for glass interposers were designed and fabricated by the advanced SAP method, and then characterized by a VNA calibrated to 20 GHz. The HFSS model with process variations correlates well with measurement data. The VNA probe landing pad deembedding method was adopted by using Matlab. The effectiveness of this method along with the cause of errors were demonstrated. The error can be avoided by using a short transmission line without the phase shift.

Finally, the 2 μm impedance controlled microstrip line design rule was provided, with the demonstration of precisely controlled 2 μm single copper trace on polymer surface.

CHAPTER 6

RESEARCH SUMMARY AND FUTURE WORK

This dissertation presented a comprehensive study of the impact of re-distribution layer (RDL) process variations on the electrical performance such as 50 ohm impedance down to 3 μm CD on glass interposers for 2.5D multi-die interconnections.

2.5D silicon interposers with high density RDL were developed using back end of line (BEOL) processes to achieve high data bandwidth logic-to-memory interconnections. Georgia Tech and others have demonstrated glass interposers as an electrically superior and large panel scalable alternative to silicon interposers. Although comprehensive process characterization and design rules have been developed to enable silicon interposer designs, there has been very limited research in understanding the impact of fabrication process variations on copper trace performance on glass interposers. The objective of this dissertation was to develop a comprehensive set of design guidelines for 2 μm RDL at 20-40μm I/O pitch by modeling, design, fabrication and characterization of copper-polymer multi-layer RDL layers on glass interposers. Although there have been a number of transmission line theories and studies on various substrates, the design guidelines for characteristic impedance tolerance in glass interposer RDLs down to 2 μm lines have not been documented.

The following fundamental challenges were identified to achieve the dissertation goals: (1) lack of a comprehensive analysis of process variation impact on electrical performance, leading to a set of design guidelines, and (2) lack of high precision panel-scale RDL processes in controlling the transmission line dimensions to achieve 50 ohm

impedance. To address the aforementioned challenges, three research tasks were carried out: (1) electrical modeling of RDLs considering fabrication process variations; (2) fabrication process development to improve routing density and line shape control using the SAP method; (3) millimeter-wave characterization of new photo-sensitive dielectric material and transmission lines to validate the electrical models.

The electrical performance analysis and process demonstration in the previous chapters prove that the research objectives were successfully met. This chapter summarizes the research outcomes of this dissertation with key scientific and technical contributions and potential future work. A list of published papers is also included.

6.1 Research Summary

6.1.1 Characteristic Impedance Controlled Fine Line RDL Design and Simulation

1. 2D extractor model: Impedance -controlled transmission line design parameters for 2.5 D glass interposers were developed for two major types of RDL processes, (a) conventional SAP, and (b) the embedded copper trace process. Ultra-thin epoxy dry films (ABF GX 92 series from Ajinomoto Japan) with 5 μm, 10 μm, and 15 μm thickness were selected for microstrip line, stripline, and CPW design with 50 Ohm impedance control at 5.8 GHz. A set of initial design rules were provided for microstrip lines and striplines with 2 μm width, 3 μm thickness, along with the required polymer dielectric material thickness to provide property targets for future material development. For microstrip line with 2 μm width and 3 μm thickness, the required effective dielectric thickness is 0.75 μm for the SAP method, and 1.09 μm for the embedded method. Both are relatively aggressive to fabricate. However, for 2 μm width and 3 μm thickness stripline, the

effective dielectric thickness is 8.36 μm, which is achievable with currently available ABF materials.

2. Process variations: Both the SAP method and embedded trace method introduce process variations, resulting in non-ideal transmission line shapes. The deviation in line shape from ideal designed parameters were analyzed for a number of key processes including copper seed layer deposition, photolithography, copper electrolytic plating, seed layer etching, and polymer trench formation. Based on these process impacts, four critical process variations for the SAP method and the embedded method were chosen to study their effect on the electrical performance of ultra-small transmission lines. These are: (1) width of copper trace, (2) thickness of copper, (3) side wall taper, and (4) copper surface roughness. For all transmission line types, reducing the copper trace width or thickness led to lower capacitance, lower conductance, higher inductance, and higher resistance, and vice versa for increasing width or thickness. The copper side wall taper angle analysis indicated that when the wider part of the trace had a width equal to the impedance controlled design value, then the tapered copper traces always had lower capacitance, lower conductance, higher inductance, and higher resistance, with unaffected conductance for SAP fabricated CPW and microstrip line as exceptions. The taper effect can be compensated by increasing the copper width, and the impedance controlled design for copper traces with tapered side walls were calculated. Even with good impedance control, the non-vertical side wall affects the RLGC in a negative direction with exceptions of microstrip lines fabricated by the embedded method. The tapered copper trace with impedance controlled design for partially embedded microstrip line showed marginally better electrical performance (0.04 dB/mm lower insertion loss at

30 GHz for around 7-8 μm width microstrip line) at the cost of wiring density. The copper surface roughness only affects the inductance and capacitance for all types of transmission lines.

3. Impedance sensitivity: The impedance sensitivity of four process variations were analyzed. For all transmission line types, a narrower signal trace than designed has higher impedance, and vice versa. The impedance sensitivity to width increases when the width reduces for microstrip line and stripline. For a SAP fabricated microstrip line with 7.5 μm designed width, the width tolerance is -8.27% to +9.2% for 5% impedance tolerance. Such width tolerance is slightly larger for a partially embedded microstrip line, which is -9.4% to +9.35% for 6.64 μm original width. For 2.94 μm stripline, the 5% impedance target yields a width tolerance of -11.8% to +13.1%. The impedance is more sensitive for CPW with narrower gap, with -6% to +5.67% width tolerance for a 3 μm width, 2.1 μm gap and 5 μm thick CPW by the SAP method to achieve a 5% impedance tolerance target. The partially embedded CPW with thinner copper thickness (2 μm) and narrow gap (1.475 μm) but same width (3 μm) has a stricter width tolerance (-4.57% to +4.53%) to achieve the same 5% impedance tolerance target. Reducing copper thickness increases the impedance of all 3 kinds of transmission lines. The impedance sensitivity is almost linear for microstrip lines within the simulated range. To be said, -12% to +12% thickness tolerance on 2 μm thick, 7.5 μm wide SAP fabricated microstrip line is necessary to control the impedance within a 5% error. This range is -11.3% to +11.25% for the embedded case. This sensitivity increases for stripline and CPW when the copper thickness decreases. For stripline's case, a 5% impedance error requires the thickness to be controlled within -9% to +11.5% for 2.94 μm width and 2 μm thick line. The tapered

copper trace leads to a higher impedance when the maximum width of the transmission line was fixed at the designed parameter. The impedance of CPW is the most sensitive to this effect. The side wall angle for SAP fabricated CPW needs to be higher than 87.7° to keep the impedance lower than 52.5 Ohm, which is a 5% increase. For a SAP fabricated microstrip line and stripline, this side wall angle is 57.7° and 80.4°, respectively. Width compensated designs can be considered if impedance control is the top priority. The copper surface roughness has the least significant impact on the impedance among all four process variations. The 0.1 μm copper surface roughness increases the impedance of all types of transmission lines by less than 3%, and 1 μm extreme rough copper increases the impedance up to 11%. However, the conductor loss is directly affected by rough conductor surfaces. The 1 μm extreme rough copper can increase the insertion loss up to 0.3 dB/mm at 30 GHz for a partially embedded microstrip line. If the insertion loss is the major concern for the specific application, the copper surface needs to be fabricated as smooth as possible.

6.1.2 Semi-Additive Process Improvements

The traditional SAP method for multi-layer RDL fabrication was improved to achieve a 2 μm line and space high density routing on glass substrates, closing the gap of the routing density between wafer foundries and package foundries.

1. Photo lithography: The photo lithography process with DFR was optimized by enhancing the adhesion between the DFR and the copper seed layer, as well as applying thinner DFR with optimized projection lithography conditions. This research led to one of the first demonstrations of 2 μm line widths using dry film resists, enabling 2 μm RDL scaling on large panels.

2. Ozone treatment: An innovative ozone treatment process was studied and implemented for SAP yield improvement in two major process steps, (a) before electrolytic copper plating and (b) after DFR stripping, as a higher throughput alternative to traditional oxygen plasma treatment. The ozone treatment cleans the organic contamination on the sample after lithography, and significantly improves the surface wettability from above a 80° water contact angle to less than a 40° contact angle, which is essential for high quality copper plating. Ozone treatment etches around 0.6 μm DFR on each side, resulting in a larger DFR trench width, which needs to be considered for precise line width control. Another application for the ozone treatment is cleaning the DFR residue after strip, for improving the overall yield of the SAP RDL.

3. Copper seed layer etch: The seed layer etch step in the SAP process flow causes significant variation in line widths as the CDs scale below 5um. Several copper seed layer etching processes were compared and analyzed for their impact on line width and shape. Compared to immersion etching, spray etching increases the vertical etching speed, resulting in less variation, while a "differential etch" chemistry (EcoFlash™ from Atotech GmbH Germany) resulted in a faster etch rate for the copper seed layer compared to the plated copper traces due to the difference in grain structure, leading to further reduction in side etching and thus improving the process control. The use of an end-point detection system (Veeco Inc.) provided a precise stopping point during the seed layer etching process, thus avoiding seed layer over-etch and potentially further reducing process variation. The spray etching method with differential etchant provided the best seed layer etch process control, with less side wall damage and a smooth copper structure

after etch. The side wall etch amount was from 0.3 μm to 0.6 μm on each side, depending on the space between traces.

4. Surface planarization: A new panel scale planarization process using Disco's surface planer tool was optimized and demonstrated to achieve uniform copper thickness across the panel, eliminating the non-uniformity of trace height caused by electrolytic copper pattern plating. Furthermore, the dielectric polymer layer can also be planarized to reduce its thickness to achieve better impedance control. A three metal layer RDL structure with 3 μm effective dielectric thickness cut from 5 μm thick ABF polymer was demonstrated by proposed surface planarization process.

5. Summary of process variations by process step: The lithography process can be optimized to achieve the same line width as the designed mask. The traditional oxygen plasma treatment increases the DFR trench width by 0.3 μm, and the novel ozone treatment increase this by 1.3 μm. The typical copper seed layer etching process reduces the line width by 0.6-1.2 μm, depending on the space between the copper traces. With the design compensations, the width variation satisfies the 5% impedance tolerance of a 2.94 μm stripline and the 10% impedance tolerance of a 2 μm microstrip line. The surface planarization process can achieve global thickness variation within 1 μm, and local control within 0.4 μm, which satisfy the impedance tolerance of 10% for 7.5 μm microstrip line and 2.94 μm stripline with 2 μm designed copper thickness. The typical copper side wall angle by SAP method is 85º, and less or equal to 100º by photo embedded method. The copper surface roughness by advanced SAP method is close to Scenario 2. Both tapered side wall and surface roughness have negligible impact on the electrical performance.

6.1.3 Millimeter-Wave Characterization of Photo-Sensitive Dielectric and Transmission Lines on Interposers

Precise measurements of dielectric constant of the polymer dielectric is another critical parameter in achieving characteristic impedance close to that of the designed value. The electrical properties of a new ultra-thin dry film photo-sensitive polymer dielectric material for via and trench formation were extracted by a modified coupling enhanced ring resonator method, and the transmission lines on glass interposer were characterized. This research demonstrated a simple de-embedding method to eliminate VNA probe landing pad effects for the high frequency characterization of ultra-fine lines.

1. Ring resonator material property extraction: Three coupling enhanced ring resonators with different first-order resonant frequencies were designed for a new ultra-thin photo-sensitive dielectric material from TOK Japan. The ring resonators were fabricated by the advanced SAP method described earlier, and measured using a high frequency VNA. An accurate and efficient method to extract the dielectric constant and loss tangent by using a 3D HFSS model was proposed and demonstrated with the measured insertion loss of the ring resonators. The extracted TOK's IF series photo-sensitive dielectric material had a relative dielectric constant of 3.1 @5.5 GHz, 3.1 @10.5 GHz, and 3.2 @15.7 GHz. The loss tangent was 0.02 @5.5 GHz, 0.03 @10.5 GHz, and 0.04 @15.7 GHz.

2. Transmission line characterization: The transmission line test structures on glass interposer were designed and fabricated by the advanced SAP method, and then characterized by a VNA calibrated to 20 GHz. The HFSS model, considering the process variations, correlated well with the measurement data. The CPW transmission line on a glass interposer was characterized and compared with that on a silicon wafer, showing

lower loss due to the insulating nature of glass. Finally, the VNA probe landing pad de-embedding method was adopted by using Matlab. The effectiveness of this method was demonstrated, and the source of small errors were identified. The errors can be avoided by using a short transmission line without a significant insertion loss phase shift.

3. Demonstration of 2 μm copper trace: With design compensation summarized from Chapter 4, a single 2 μm wide copper trace with precision control was demonstrated. The measured actual width was 2.1 μm, which satisfies the 2 μm microstrip line design rule with the 5% impedance tolerance. The ultra-thin dielectric polymer required for 2 μm microstrip line requires future work.

6.2 Key Contributions

The key contributions of this dissertation are summarized below:

- Developed a comprehensive set of impedance matched RDL trace design rules for glass interposers based on available dielectric polymers with different thicknesses, as well as 2 μm line dimensions.
- Conducted a parametric study of the impact of four major fabrication process variations on the parasitic RLGC of three common types of transmission lines for the first time. Most of the process variations negatively affect the electrical performance, except the impedance controlled microstrip lines fabricated by the embedded trace process with tapered side walls. The tapered side wall slightly improves the electrical performance, at the cost of wiring density.
- Investigation of line shape tolerance of three common types of transmission lines based on different characteristic impedance targets using 2D extractor models in Ansoft Electromagnetic Suite to provide design guidelines for precise impedance control.

- High resolution panel scale lithography process advances for ultra-fine feature patterning with dry-film resist, enabling high aspect ratio 2 μm line and space routing.
- First demonstration of ozone treatment process as a higher throughput alternative to traditional plasma treatment for surface wettability modification and cleaning, improving the copper plating quality and yield, as well as photoresist residue removal at 2 μm CD.
- Demonstration of a novel differential seed layer etching technique to reduce the copper side wall etch and undercut, improving the overall yield and impedance control using the SAP method for ultra-fine RDL fabrication
- A cost effective, panel scale, surface planarization process was optimized and integrated into multi-layer RDL fabrication for better process control. The dielectric polymer was thinned down by the same process for the first time to meet the impedance control requirements.
- New coupling enhanced ring resonators were designed for a new class of photo-sensitive dielectric materials from TOK. The dielectric constant and loss tangent were extracted by the HFSS model with excellent correlation to the VNA measurements.
- Different transmission lines were fabricated on glass interposers by the proposed advanced SAP method. The HFSS models factoring in the process variations correlated well with the VNA measurement results.
- A simple de-embedding method to eliminate the VNA probe landing pad effect was proposed and demonstrated by using S-parameter bi-section algorithms.
- A single 2 μm wide copper trace with precise width control was demonstrated by the advanced SAP method with the design compensation for the first time.

6.3 Future Work

The objective of this dissertation was to develop a thorough understanding of the impact of RDL process variations on the electrical performance of impedance controlled

transmission lines at 2 μm CDs on 2.5D glass interposers. This research focused on the electrical model analysis on single ended transmission lines and SAP process advances. Beyond the focus of this dissertation, there are a number of research topics that can be investigated to further improve the performance and expand the applications of 2.5D glass interposers, as discussed below:

Ultra-thin Dielectric with Precise Thickness Control

The dielectric polymer thickness control is critical for a strict impedance target. An improved surface planarization process is required to achieve ±0.1 μm thickness accuracy of the ultra-thin polymer for a 2 μm microstrip line with a 5% impedance tolerance.

Differential Pair Modeling

Differential signaling is very common in a package where high speed and electromagnetic interference (EMI) rejection is required. If balanced, no current flows though the return path (ground plane), which minimizes power integrity issues. The same process impact on the impedance of differential transmission line pairs needs to be systematically analyzed to provide the design guidelines for differential signaling in glass interposers.

Embedded Process Development

Although this dissertation demonstrated an advanced SAP method, the seed layer etching step will inevitably roughen and etch the copper traces. To compensate the copper trace width shrinkage due to seed layer etching, the metallized copper traces before seed layer etching have to be wider than the target design dimensions. However,

wider copper traces may result in narrow line-to-line gaps, resulting in smaller CD during the photolithography process. The embedded trench processes overcome the limitations of the SAP method similar to the dual damascene process applied in wafer level RDL processes. Thin-film photo-sensitive dielectric materials are ideal for small trench and via formation. The resolution of this material determines the minimum RDL line and space. Such an embedded trench process has better width control than SAP method by eliminating the seed layer etching step. However, photoresists typically used for the SAP method tend to have higher resolution than photo-imageable dielectric (PID) polymers, and there is a need for further advances in dry film PID materials.

Embedded Trace Electrical Characterization

The current generation photo-sensitive dielectric is relatively lossy at high frequencies, according to the microstrip line characterization in Chapter 5. Although current wide I/O interconnections have low signal speeds in the few hundred Mbps to 1Gbps range, the roadmaps for high bandwidth logic-memory integration call for multiple Gbps signaling in wide I/O channels. Higher line aspect ratios will be required in the future to reduce the line resistance and enable higher channel speeds. Transmission lines fabricated by the embedded trench process have yet to be characterized and correlated to EM models to enable its use for wide I/O 2.5D interposers.

6.4 Publications

6.4.1 Peer-reviewed Journals

1. **Hao Lu**, Ryuta Furuya, Brett Sawyer, Chandrasekharan Nair, Fuhan Liu, Venky Sundaram, and Rao Tummala, “Design, Modeling, Fabrication and

Characterization of 2-5 Micron Redistribution Layer Traces by Advanced Semi-Additive Processes on Low Cost Panel-Based Glass Interposers," *IEEE Trans. Compon. Packag. Manuf. Technol*., vol. 6, issue 6, pp. 959-967, 2016.

2. Qiao Chen, **Hao Lu**, Venky Sundaram, and Rao Tummala, "Modeling, Fabrication, and Reliability of Through Vias in Polycrystalline Silicon Panels," *IEEE Trans. Compon. Packag. Manuf. Technol*., vol. 5, issue 7, pp. 938-944, 2015.
3. Brett Sawyer, Yuya Suzuki, Zihan Wu, **Hao Lu**, Venky Sundaram, Kadappan Panayappan, and Rao Tummala, "Design and Demonstration of 40 Micron Bump Pitch Multi-layer RDL on Panel-Based Glass Interposers," *Journal of Microelectronics and Electronic Packaging*, vol. 13, issue 3, pp. 128-135, 2016.
4. **Hao Lu**, Venky Sundaram, and Rao Tummala, "Design and Modeling of Impedance Controlled Multilayer RDL on Glass Interposer with Fabrication Process Variations," submitted to *IEEE Trans. Compon. Packag. Manuf. Technol*.
5. **Hao Lu**, Kadappan Panayappan, Venky Sundaram and Rao Tummala, "Characterization of the Effect of RDL Process Variations on the Design of Highly Precise Impedance Controlled Transmission Lines on Glass Interposers", in preparation.

6.4.2 Conference Proceedings

1. **Hao Lu**, Yutaka Takagi, Yuya Suzuki, Brett Sawyer, Robin Taylor, Venky Sundaram, and Rao Tummala, "Demonstration of 3-5 μm RDL Line Lithography on Panel-Based Glass Interposers," in *Proc. IEEE 64th ECTC*, 2014, pp. 1416-1420.

2. **Hao Lu**, Frank Wei, Ryuta Furuya, Atsushi Kubo, Fuhan Liu, Venky Sundaram, Rao Tummala, "Advances in Panel Scalable Planarization and High Throughput Differential Seed Layer Etching Processes for Multilayer RDL at 20 Micron I/O Pitch for 2.5D Glass Interposers," in *Proc. IEEE 66th ECTC*, 2016, pp. 2210-2215.
3. Brett Sawyer, **Hao Lu**, Yuya Suzuki, Yutaka Takagi, Makoto Kobayashi, Vanessa Smet, Taiji Sakai, Venky Sundaram, and Rao Tummala, "Modeling, Design, Fabrication, and Characterization of First Large 2.5D Glass Interposer as a Superior Alternative to Silicon and Organic Interposers at 50 Micron Bump Pitch," in *Proc. IEEE 64th ECTC*, 2014, pp. 742-747.
4. Ryuta Furuya, **Hao Lu**, Fuhan Liu, Hai Deng, Tomoyuki Ando, Venky Sundaram, and Rao Tummala, "Demonstration of 2 μm RDL Wiring Using Dry Film Photoresists and 5 μm RDL Via by Projection Lithography for Low-Cost 2.5D Panel-Based Glass and Organic Interposers," in *Proc. IEEE 65th ECTC*, 2015, pp. 1488-1493.
5. Chandrasekharan Nair, **Hao Lu**, Kadappan Panayappan, Fuhan Liu, Venky Sundaram, and Rao Tummala, "Effect of Ultra-Fine Pitch RDL Process Variations on the Electrical Performance of 2.5D Glass Interposers up to 110 GHz," in *Proc. IEEE 66th ECTC*, 2016, pp. 2408-2413.
6. Venky Sundaram, Qiao Chen, Tao Wang, **Hao Lu**, Yuya Suzuki, Vanessa Smet, Makoto Kobayashi, Raj Pulugurtha, and Rao Tummala, "Low Cost, High Performance, and High Reliability 2.5D Silicon Interposer," in *Proc. IEEE 63th ECTC*, 2013, pp. 342-347.

7. P Markondeya Raj, Chandrasekharan Nair, **Hao Lu**, Fuhan Liu, Venky Sundaram, Dennis W Hess, and Rao Tummala, " 'Zero-Undercut' Semi-Additive Copper Patterning - a Breakthrough for Ultrafine-Line RDL Lithographic Structures and Precision RF Thinfilm Passives," in *Proc. IEEE 65th ECTC*, 2015, pp. 402-405.
8. Taiji Sakai, Brett Sawyer, **Hao Lu**, Yutaka Takagi, Ryuta Furuya, Yuya Suzuki, Makoto Kobayashi, Vanessa Smet, Venky Sundaram, and Rao Tummala, "Design and Demonstration of Large 2.5D Glass Interposer for High Bandwidth Applications," in *IEEE CPMT Symposium Japan (ICSJ)*, 2014, pp. 138-141.
9. Atsushi Kubo, Chandrasekharan Nair, Ryuta Furuya, Tomoyuki Ando, **Hao Lu**, Fuhan Liu, Venky Sundaram, and Rao Tummala, "Demonstration of 20 μm I/O Pitch RDL Using a Novel, Ultra-Thin Dry Film Photosensitive Dielectric for Panel-Based Glass Interposers," in *Proc. IEEE 66th ECTC*, 2016, pp. 172-177.
10. Fuhan Liu, Chandrasekharan Nair, Atsushi Kubo, Tomoyuki Ando, **Hao Lu**, Rui Zhang, Hang Chen, Kwon Sang Lee, Venky Sundaram, and Rao Tummala, "Via-in-Trench: A Revolutionary Panel-Based Package RDL Configuration Capable of 200-450 IO/mm/Layer, an Innovation for More-Than-Moore System Integration," in *Proc. IEEE 67th ECTC*, 2017, pp. 2097-2193.
11. Atul Gupta, Eric Snyder, Christiane Gottschalk, Kevin Wenzel, James Gunn, **Hao Lu**, Yuya Suzuki, Venky Sundaram, and Rao Tummala, "First Demonstration of Photoresist Cleaning for Fine-Line RDL Yield Enhancement by an Innovative Ozone Treatment Process for Panel Fan-Out and Interposers," in *Proc. IEEE 67th ECTC*, 2017, pp. 609-614.

12. Frank Wei, Vanessa Smet, Ninand Shahane, **Hao Lu**, Venky Sundaram, and Rao Tummala, "Ultra-Precise Low-Cost Surface Planarization Process for Advanced Packaging Fabrications and Die Assembly: A Survey of Recent Investigations on Unit Process Applications and Integrations," in *Proc. IEEE 66th ECTC*, 2016, pp. 1740-1745.

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